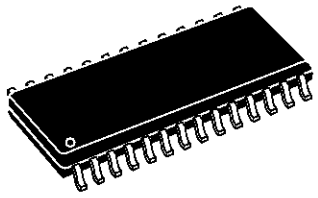
SGS-THOMSON MICROELECTRONICS

STV0118

PAL/NTSC HIGH PERFORMANCE DIGITAL ENCODER

PRELIMINARY DATA

- **NTSC-M, PAL-B, D, G, H, I, N, M, PLUS NTSC-4.43 ENCODING** (OPTIONAL PEDESTAL IN ALL STANDARDS)
- **SMALL AND ECONOMICAL SO28 PACKAGE**
- **LINE SKIP/INSERT CAPABILITY SUPPRESSING THE NEED FOR AN EXTERNAL VCXO, THUS REDUCING APPLICATION COST**
- **4 SIMULTANEOUS ANALOG OUTPUTS : RGB + CVBS, or S-VHS (Y/C) + CVBS1 + CVBS2**
- **54MHz INPUT MULTIPLEX INTERFACE FOR DOUBLE ENCODING APPLICATIONS** (TO BE ABLE TO ENCODE OR NOT THE OSD CONTENT OF THE VIDEO INPUT STREAM)
- **CROSS-COLOR REDUCTION BY SPECIFIC TRAP FILTERING ON LUMA WITHIN CVBS FLOW**
- **CLOSED CAPTIONING, CGMS ENCODING AND TELETEXT ENCODING**
- ITU-R/CCIR601 ENCODING WITH EASILY PROGRAMMABLE COLOR SUB-CARRIER FREQUENCIES
- DIGITAL FRAME SYNC INPUT/OUTPUT (ODDEV/VSYNC), PROGRAMMABLE POLARITY AND RELATIVE POSITION
- DIGITAL HORIZONTAL SYNC INPUT/OUPUT (HSYNC), PROGRAMMABLE POLARITY AND RELATIVE POSITION
- DIGITAL LINE OR FRAME SYNC EXTRACTION FROM ITU-R/CCIR656 / D1 DATA
- MASTER OPERATION MODE, PLUS 6 SLAVE MODES
- INTERLACED/NON-INTERLACED OPERATION MODES
- FULL OR PARTIAL VERTICAL BLANKING
- LUMA FILTERING WITH 2X OVERSAMPLING & SINY/Y CORRECTION
- CHROMINANCE FILTERING WITH 4X OVERSAMPLING TO EITHER 1.1MHz, 1.3MHz, 1.6MHz or 1.9MHz
- WIDE CHROMINANCE BANDWIDTH FOR RGB ENCODING (2.45MHz)
- 24-BIT DIRECT DIGITAL FREQUENCY SYNTHESIZER FOR COLOR SUBCARRIER
- PROGRAMMABLE RESET OF COLOR SUBCARRIER PHASE (4 MODES)
- EASY CONTROL VIA FAST I^2C BUS
- TWO I^2C ADDRESSES
- AUTOTEST OPERATION MODE (ON-CHIP COLOR BAR PATTERN 100/0/75/0)
- CMOS TECHNOLOGY WITH 3.3V POWER SUPPLY
- APPLICATIONS : SATELLITE, CABLE & TERRESTRIAL DIGITAL TV DECODERS, MULTIMEDIA TERMINALS, DVD PLAYERS



SO28
(Plastic Micropackage)

ORDER CODE : STV0118

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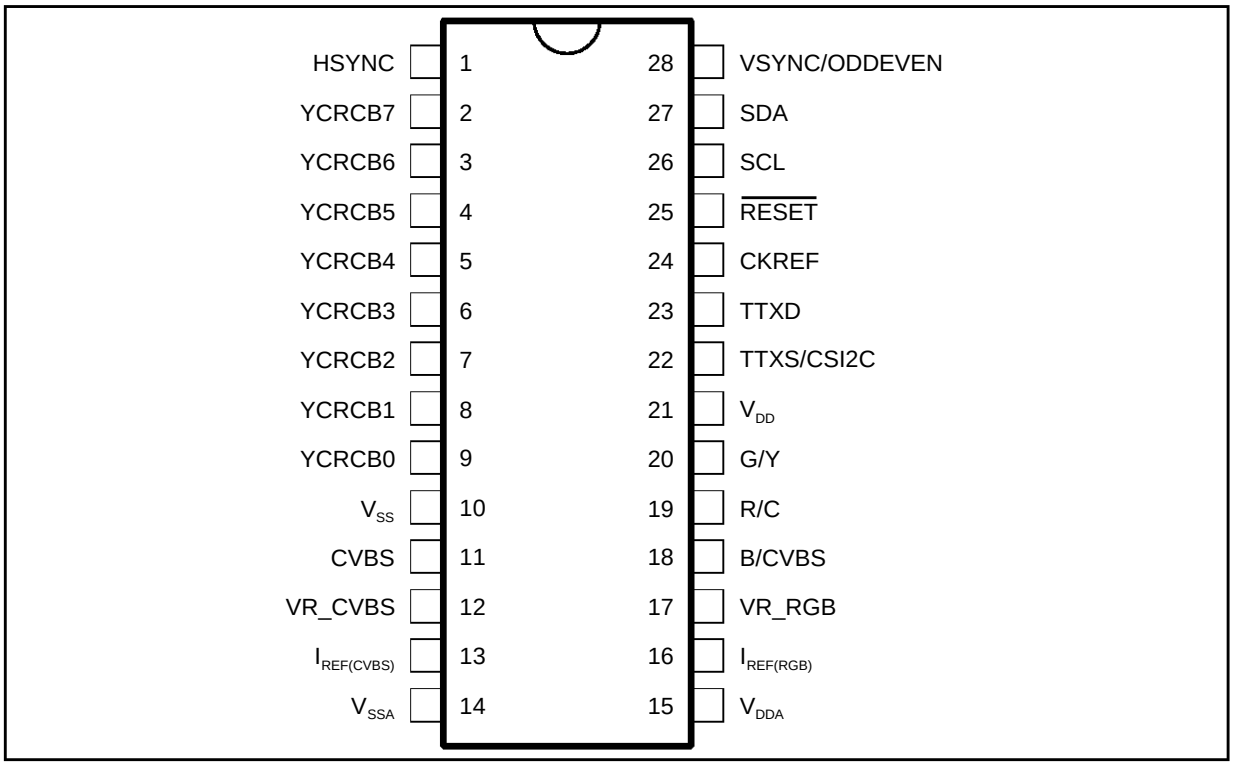
I - GENERAL DESCRIPTION

The STV0118 is a high performance PAL/NTSC digital encoder in a low cost pakage. It converts a 4:2:2 digital video stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The STV0118 can handle interlaced mode (with 525/625 line standards) and non-interlaced mode. It can perform Closed-Captions, CGMS or Teletext encoding.

Four analog output pins are available, on which it is possible to output either S-VHS(Y/C) + CVBS1 + CVBS2 or RGB + CVBS. Moreover, it is possible to use two STV0118 in parallel to interface with SGS-THOMSON's MPEG decoder ICs that are able to deliver a 54Mbit/s "double" YCrCb stream (e.g. the STi3520M). This allows for example to encode OSD in one of the streams only.

II - PIN INFORMATION

II.1 - Pin Connections



II - PIN INFORMATION (continued)

II.2 - Pin Description

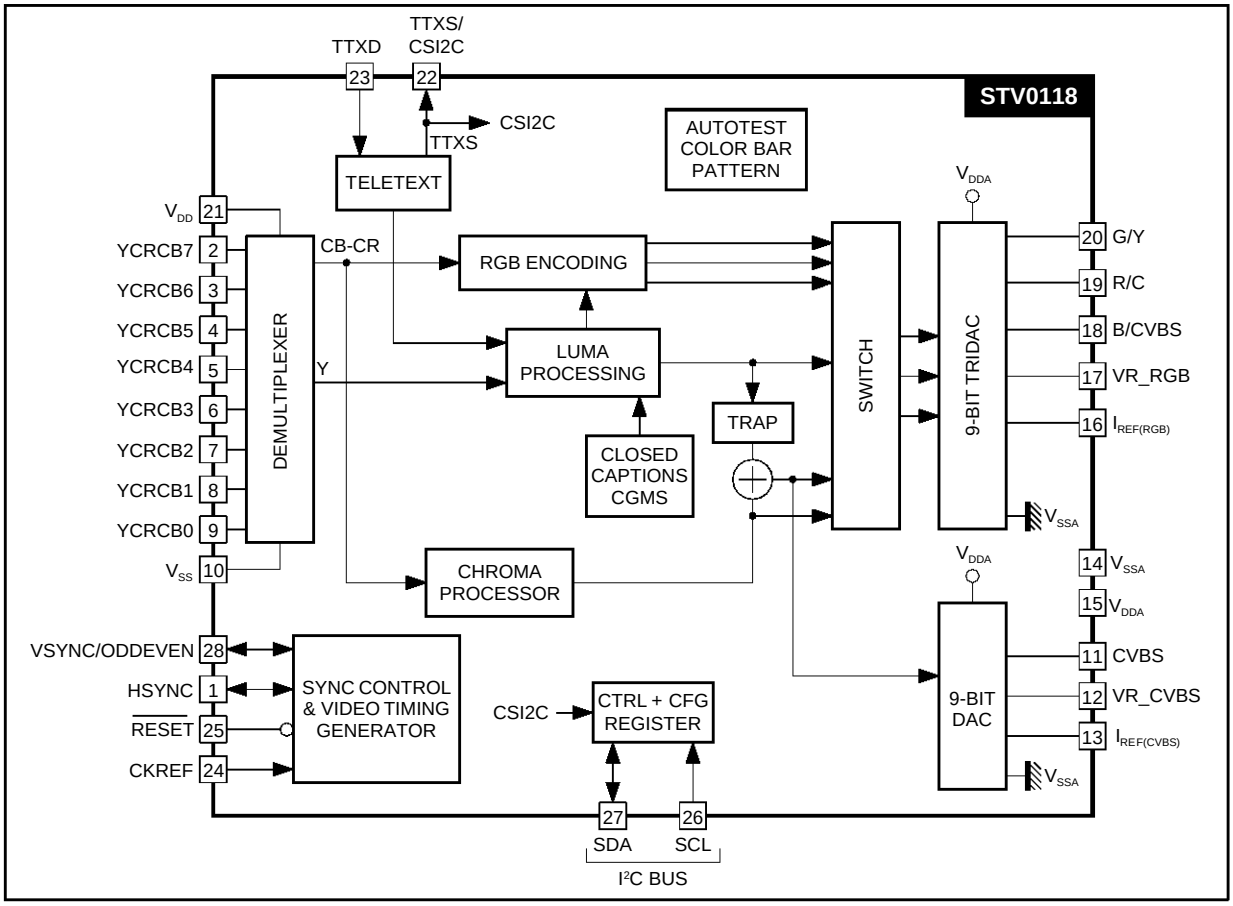
Pin	Name	Type	Function
1	HSYNC	I/O	Line Synchronization Signal : - Input in ODDEV+HSYNC or VSYNC + HSYNC or VSYNC slave modes - Output in all other modes (master/slave) - Synchronous to rising edge of CKREF - Default polarity : negative pulse
2 3 4 5 6 7 8 9	YCrCb7 YCrCb6 YCrCb5 YCrCb4 YCrCb3 YCrCb2 YCrCb1 YCrCb0	I/O I/O I/O I/O I/O I/O I/O I/O	Input : time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus interfaces with MPEG video decoder output port and typically carries a stream of Cb,Y,Cr,Y digital video at CKREF frequency, clocked on the rising edge (by default) of CKREF. A 54-Mbit/s 'double' Cb, Y, Cr, Y input multiplex is supported for double encoding application (rising and falling edge of CKREF are operating). Output: for test purpose only.
10	V_{SS}	Supply	Digital Ground
11	CVBS	Output	Analog Composite Video Output (current-driven). CVBS must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended CVBS amplitude is proportional to $I_{REF(CVBS)}$ ($V_{OUT(N)} = N \times R_{LOAD} \times I_{REF(CVBS)}/96$) with N = [0-511] $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$
12	VR_CVBS	I/O	Internal Reference Voltage for the 9-bit DAC CVBS. VR_CVBS must be connected to analog ground over a capacitor (6.8nF typ.), VR_CVBS = 1.9V
13	$I_{REF(CVBS)}$	I/O	Reference current source for the 9-bit DAC CVBS. - $I_{REF(CVBS)}$ must be biased to analog ground over a reference resistor $R_{REF(CVBS)}$ - $R_{REF(CVBS)(Min.)} = 5.95 \times R_{LOAD}/V_{OUT(Max.)}$ with $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$ ($I_{REF(CVBS)} = V_{REF(CVBS)}/R_{REF(CVBS)}$), $V_{REF(CVBS)(Typ.)} = 1.12V$.
14	V_{SSA}	Supply	Analog ground for DACs
15	V_{DDA}	Supply	Analog positive power supply for DACs (+3.3V nom.)
16	$I_{REF(RGB)}$	I/O	Reference current source for Tri-DAC R/Y,G/C,B/CVBS. -$I_{REF(RGB)}$ must be connected to analog ground over a reference resistor $R_{REF(RGB)}$ -$R_{REF(RGB)(Min.)} = 5.95 \times R_{LOAD}/V_{OUT(Max.)}$, with $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$ ($I_{REF(RGB)} = V_{REF(RGB)}/R_{REF(RGB)}$), $V_{REF(RGB)(Typ.)} = 1.12V$.
17	VR_RGB	I/O	Internal reference voltage for the 9bit Tri-DAC R/Y,G/C,B/CVBS. VR_RGB must be biased to analog ground over a typical 6.8nF capacitor, VR_RGB = 1.9V.
18	B/CVBS	O	Analog 'Blue' or CVBS output (current-driven). This output must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$ ($V_{OUT(N)} = N \times R_{LOAD} \times I_{REF(RGB)}/96$) with N = [0-511].
19	R/C	O	Analog 'Red' or S-VHS Chrominance output (current-driven). This output must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$ ($V_{OUT(N)} = N \times R_{LOAD} \times I_{REF(RGB)}/96$) with N = [0-511].
20	G/Y	O	Analog 'Green' or S-VHS Luminance output (current-driven). This output must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. $V_{OUT(Max.)} = 1V_{PP}$ and $I_{OUT(Max.)} = 5mA$ ($V_{OUT(N)} = N \times R_{LOAD} \times I_{REF(RGB)}/96$) with N = [0-511].
21	V_{DD}	Supply	Digital positive supply voltage (+3.3V nom.)
22	TTXS/CSI2C	I/O	Output : positive sync pulse for control of Teletext buffer in external demultiplexer or Transport IC.
23	TTXD	I/O	Teletext data stream from external demultiplexer or Transport IC synchronous to rising edge of CKREF signal average rate of 6.9375Mbit/s. Output in test mode only.

II - PIN INFORMATION (continued)

II.2 - Pin Description (continued)

Pin	Name	Type	Function
24	CKREF	I	Master clock reference signal. Its rising edge is the default reference for set-up and hold times of all inputs, and for propagation delay of all outputs (except for SDA output). CKREF nominal frequency is 27MHz (CCIR601) : input pad with pull down (50kΩ Typ.)
25	$\overline{\text{RESET}}$	I	Hardware reset, active LOW. It has priority over software reset. NRESET imposes default states (see Register Contents). Minimum Low level required duration is 5 CKREF periods : input pad with pull down (50kΩ Typ.)
26	SCL	I	I^2C bus clock line (internal 5-bit majority logic with CKREF for reference) : input pad with pull down (50kΩ Typ.)
27	SDA	I/O	I^2C bus serial data line. Input : internal 5-bit majority logic with CKREF for reference Output : open drain
28	VSYNC/ ODDEVEN	I/O	Frame sync signal : - input in slave modes, except when sync is extracted from YCrCb data - output in master mode and when sync is extracted from YCrCb data - synchronous to rising edge of CKREF - ODDEVEN default polarity : odd (not-top) field : LOW level even (bottom) field : HIGH level

III - BLOCK DIAGRAM



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IV - FUNCTIONAL DESCRIPTION

The STV0118 can operate either in master mode, where it supplies all sync signals, or in 6 slave modes, where it locks onto incoming sync signals.

The main functions are controlled by a micro-controller via an I^2C 2-wire bus. Refer to the "User's Register Description" for an exhaustive list of the control possibilities available.

IV.1 - Data Input Format

The digital input is a time-multiplexed ITU-R656 /D1-type [Cb, Y, Cr, Y] 8-bit stream. Note that "ITU-R" was formerly known as "CCIR". Input samples are latched in on the rising edge (by default) of the clock signal CKREF, whose nominal frequency is 27MHz. Figure 1 illustrates the expected data input format. Alternatively, a 54-Mbit/s stream can be fed to the STV0118, refer to Section IV.17 ("dual encoding") for details.

The STV0118 is able to encode interlaced and non-interlaced video. One bit is sufficient to automatically direct the STV0118 to process non-interlaced video. Update is performed internally on the first frame sync active edge following the programming of this bit. The non-interlaced mode is a 624/2 = 312 line mode or a 524/2 = 262 line mode, where all fields are identical.

An 'autotest' mode is available by setting 3 bits (sync[2:0]) within the configurations register0. In this mode, a color bar pattern is produced, independently from video input, in the adequate standard. As this mode sets the STV0118 in master mode, VSYNC/ODDEV and HSYNC pins are then in output mode.

IV.2 - Video Timing

The STV0118 outputs interlaced or non-interlaced video in PAL-B, D, G, H, I, PAL-N, PAL-M or NTSC-M standards and 'NTSC- 4.43' is also possible.

The 4-frame (for PAL) or 2 frame (for NTSC) burst sequences are internally generated, subcarrier generation being performed numerically with CKREF as reference. Rise and fall times of synchronization tips and burst enveloppe are internally controlled according to the relevant ITU-R and SMPTE recommendations.

Figures 2 to 7 depict typical VBI waveforms.

It is possible to allow encoding of incoming YCrCb data on those lines of the VBI that do not bear line sync pulses or pre/post-equalisation pulses (see Figures 2 to 7). This mode of operation is refered to as "partial blanking" and is the default set-up. It allows to keep in the encoded waveform any VBI data present in digitized form in the incoming YCrCb stream (e.g. WSS data, VPS, supplementary Closed-Captions line or StarSight data, etc.). Alternatively, the complete VBI may be blanked (no incoming YCrCb data encoded on these lines, "full blanking").

The complete VBI comprises of the following lines :
- for 525/60 systems (SMPTE line numbering convention) : lines 1 to 19 and second half of line 263 to line 282.
- for 625/50 systems (CCIR line numbering convention) : second half of line 623 to line 22 and lines 311 to 335.

The 'partial' VBI consists of :
- for 525/60 systems (SMPTE line numbering convention) : lines 1 to 9 and second half of line 263 to line 272.
- for 625/50 systems (CCIR line numbering convention) : second half of line 623 to line 5 and lines 311 to 318.

Full or partial blanking is controlled by configuration bit 'blkli in configuration register1'.

Note that :
- line 282 in 525/60/SMPTE systems is either fully blanked or fully active.
- line 23 in 625/60/CCIR systems is always fully active.

In an ITU-R656-compliant digital TV line, the active portion of the digital line is the portion included between the SAV (Start of Active Video) and EAV (End of Active Video) words. However, this digital active line starts somewhat earlier and may end slightly later than the active line usually defined by analog standards. The STV0118 allows two approaches :
- It is possible to encode the full digital line (720 pixels / 1440 clock cycles). In this case, the output waveform will reflect the full YCrCb stream included between SAV and EAV.
- Alternatively, it is possible to drop some YCrCb samples at the extremities of the digital line so that the encoded analog line fits within the 'analog' ITU-R/SMPTE specifications.

Selection between these two modes of operation is performed with bit 'aline' in configuration register 4.

In all cases, the transitions between horizontal blanking and active video are shaped to avoid too steep edges within the active video. Figure 8 gives timings concerning the horizontal blanking interval and the active video interval.

IV - FUNCTIONAL DESCRIPTION (continued)

Figure 1 : Input Data Format

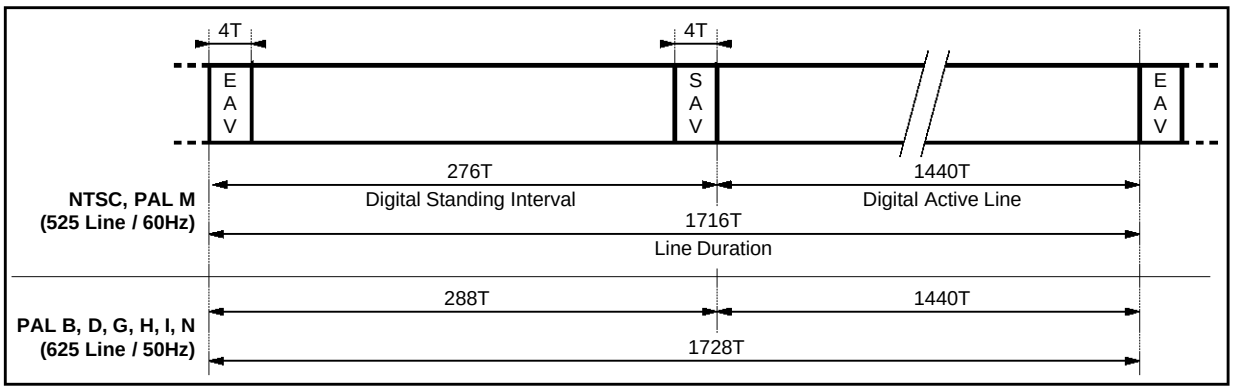


Figure 2 : PAL-BDGHI, PAL-N Typical VBI Waveform, Interlaced Mode (CCIR-625 Line Numbering)

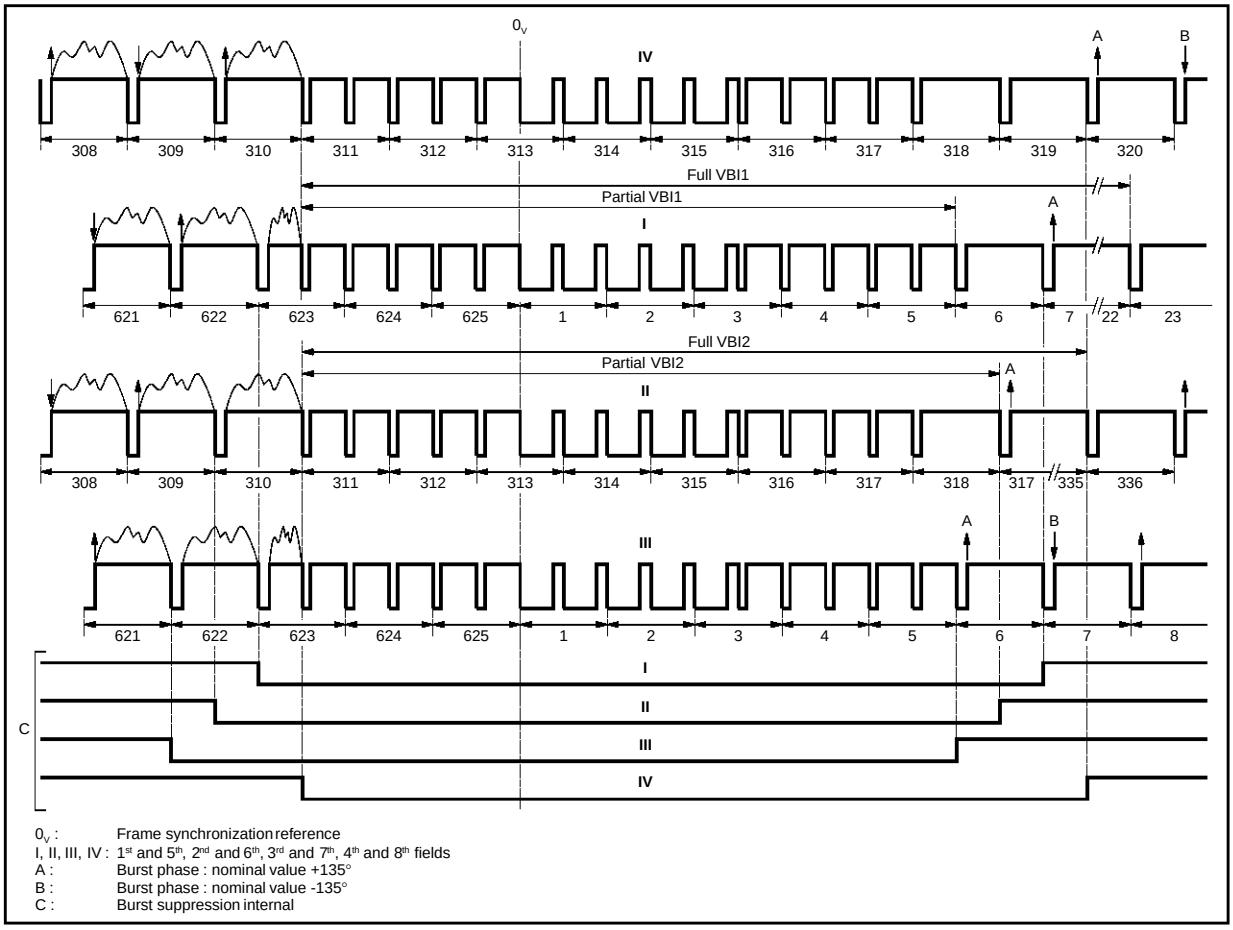
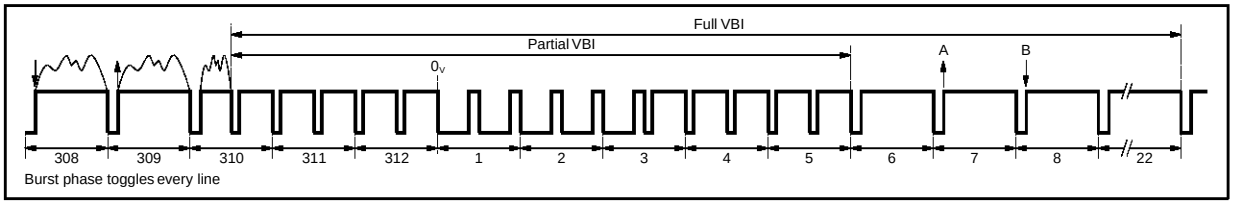


Figure 3 : PAL-BDGHI, PAL-N Typical VBI Waveform, Non-interlaced Mode ("CCIR-like" Line Numbering)



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 4 : NTSC-M Typical VBI Waveforms, Interlaced Mode (SMPTE-525 Line Numbering)

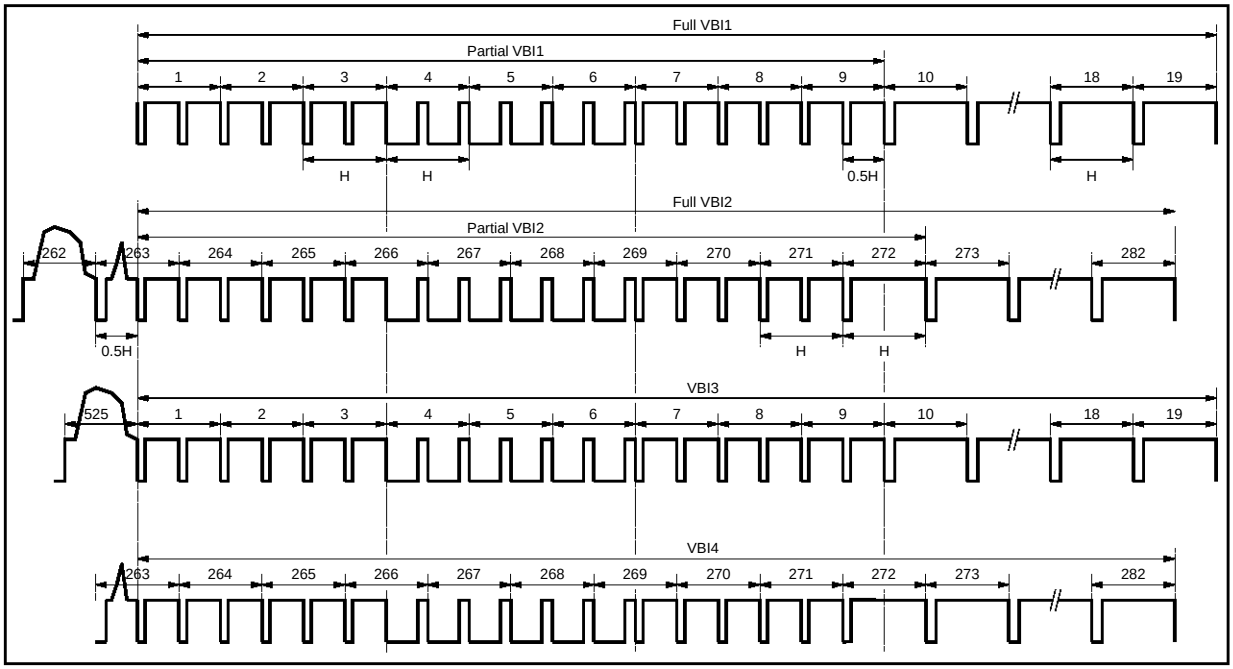
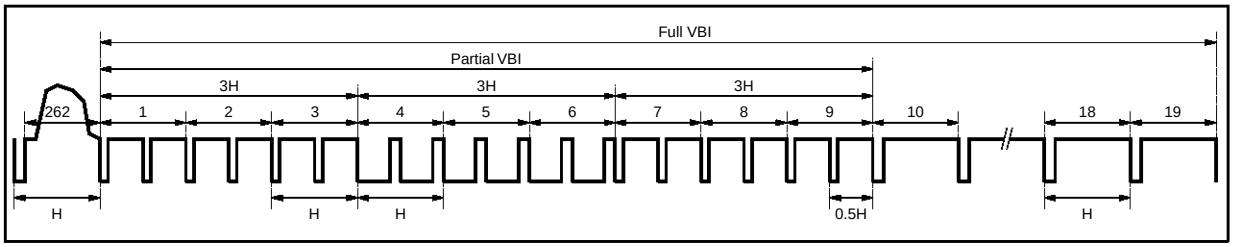


Figure 5 : NTSC-M Typical VBI Waveforms, Non-interlaced Mode ("SMPTE-like" Line Numbering)



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 6 : PAL-M Typical VBI Waveforms, Interlaced Mode (CCIR-525 Line Numbering)

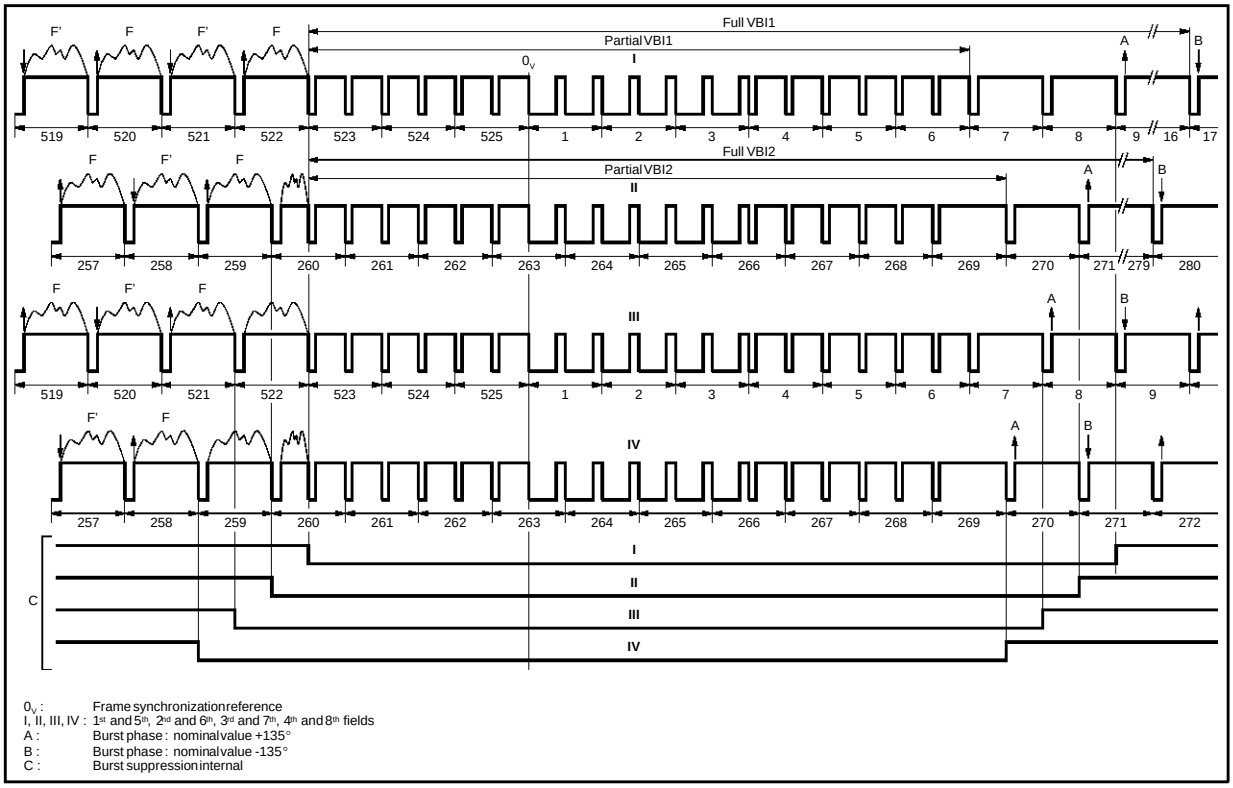
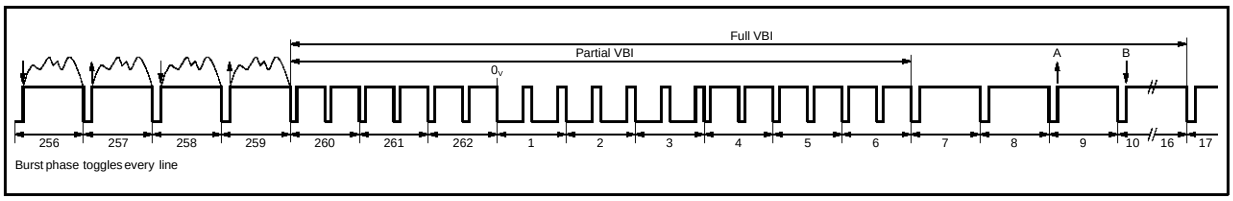
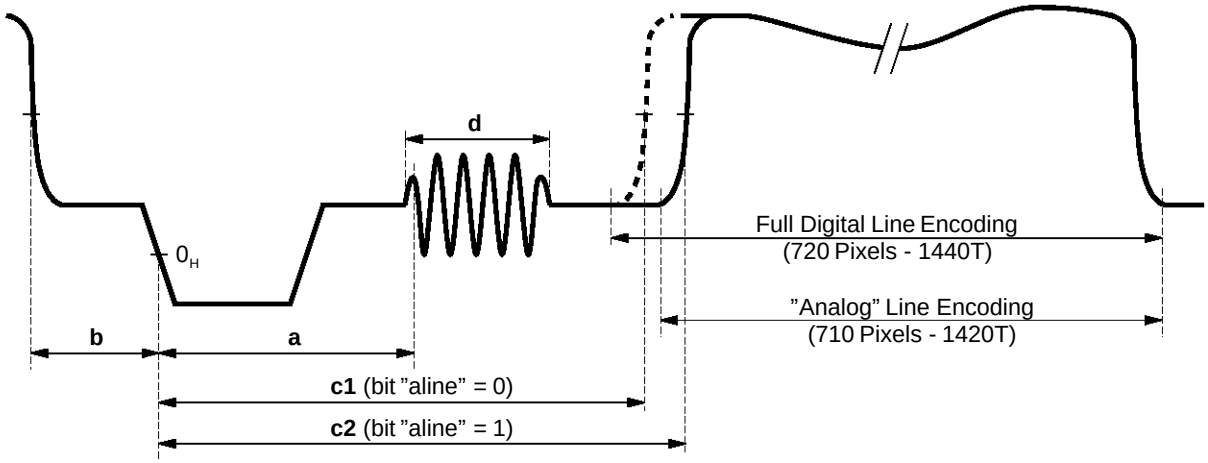


Figure 7 : PAL-M Typical VBI Waveforms, Non-interlaced Mode ("CCIR-like" Line Numbering)



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 8 : Horizontal Blanking Interval and Active Video Timings



	NTSC-M	PAL-BDGHI	PAL-N	PAL-M
a	5.38µs (even lines) 5.52µs (odd lines)	5.54µs (A-type) 5.66µs (B-type)	5.54µs (A-type) 5.66µs (B-type)	5.73µs (A-type) 5.87µs (B-type)
	These are typical values. Actual values will depend on the static offset programmed for subcarrier generation.			
b	1.56µs	1.28µs	1.28µs	1.28µs
c1	8.8µs	9.3µs	9.3µs	9.3µs
c2	9.3µs	10.1µs	10.1µs	10.1µs
d	9 Cycles of 3.58MHz	10 Cycles of 4.43MHz	9 Cycles of 3.58MHz	9 Cycles of 3.58MHz

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IV.3 - Reset Procedure

A hardware reset is performed by grounding the pin NRESET. The master clock must be running and pin NRESET kept low for a minimum of 5 clock cycles. This sets the STV0118 in HSYNC+ODDEV (line-locked) slave mode, for NTSC-M, interlaced ITU-R601 encoding. Closed-captioning and Teletext encoding are all disabled.

Then the configuration can be customized by writing into the appropriate registers. A few registers are never reset, their contents is unknown until the first loading (refer to the Register Contents and Description).

It is also possible to perform a software reset by setting bit'softreset' in Reg 6. The IC's response in that case is similar to its response after a hardware reset, except that Configuration Registers (Reg 0 to 6) and a few other registers (see description of bit 'softreset') are not altered .

IV - FUNCTIONAL DESCRIPTION (continued)

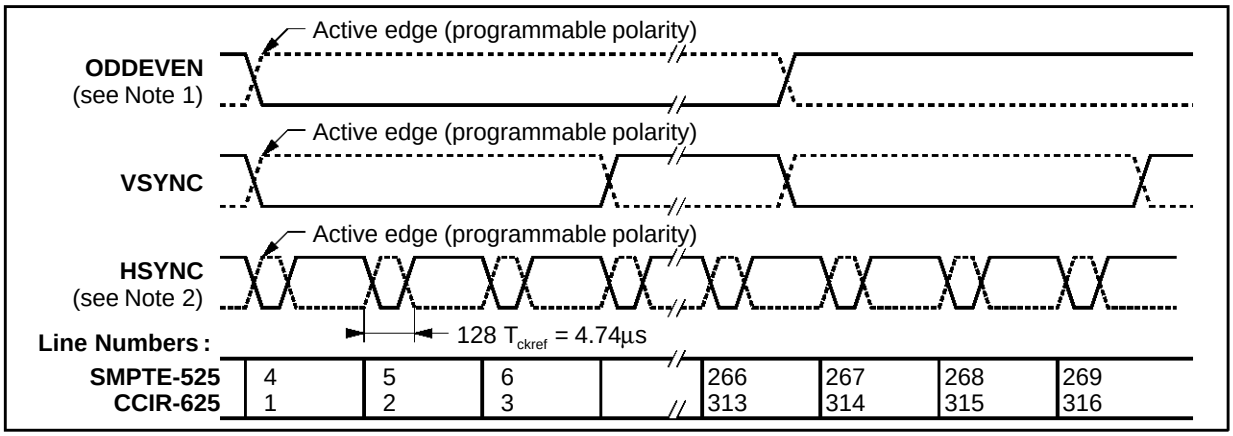
IV.4 - Master Mode

In this mode, the STV0118 supplies HSYNC and ODDEV sync signals (with independently programmable polarities) to drive other blocks. Refer to Figure 9 and 10 for timings and waveforms.

The STV0118 starts encoding and counting clock cycles as soon as the master mode has been loaded into the control register (Reg.0).

Configuration bits "Syncout_ad[1:0]" (Reg4) allow to shift the relative position of the sync signals by up to 3 clock cycles to cope with any YCrCb phasing.

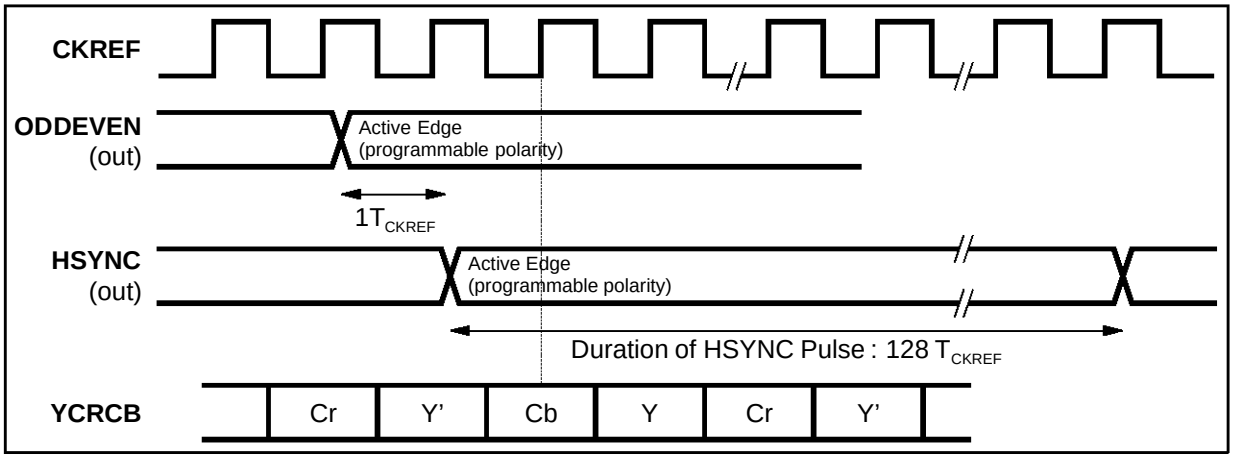
Figure 9 : ODDEVEN, VSYNC and HSYNC Waveforms



Notes : 1. When ODDEVEN is a sync input, only one edge ("the active edge") of the incoming ODDEVEN is taken into account for synchronization. The "non-active" edge (2nd edge on this drawing) is not critical and its position may differ by H/2 from the location shown.

2. The HSYNC pulse width indicated is valid when the STV0118 supplies HSYNC. In those slave modes where it receives HSYNC, only the edge defined as active is relevant, and the width of the HSYNC pulse it receives is not critical.

Figure 10 : Master Mode Sync Signals



Note : 1. This figure is valid for bits "syncout_ad[1Ø]" = default.

IV - FUNCTIONAL DESCRIPTION (continued)

IV.5 - Slave Modes

Six slave modes are available : ODDEV+HSYNC based (line-based sync), VSYNC+HSYNC based (another type of line-based sync), ODDEV-only based (frame-based sync), VSYNC-only based (another type of frame-based sync), or sync-in-data based (line locked or frame locked).

ODDEV refers to an odd/even (also known as not-top/bottom) field flag, HSYNC is a line sync signal, VSYNC is a vertical sync signal. Their waveforms are depicted in Figure 9. The polarities of HSYNC and VSYNC/ODDEV are independently programmable in all slave modes.

IV.5.1 - Synchronization onto a Line Sync Signal

IV.5.1.1 - HSYNC+ODDEV Based Synchronization

Synchronization is performed on a line-by-line basis by locking onto incoming ODDEV and HSYNC signals. Refer to Figure 11 for waveforms and timings. The polarities of the active edges of HSYNC and ODDEV are programmable and independent.

The first active edge of ODDEV initializes the internal line counter but encoding of the first line does not start until an HSYNC active edge is detected (at the earliest, HSYNC may transition at the same time as ODDEV). At that point, the internal sample counter is initialized and encoding of the first line starts. Then, encoding of each subsequent line is individually triggered by HSYNC active edges. The phase relationship between HSYNC and the incoming YCrCB data is normally such that the first clock rising edge following the HSYNC active edge samples “Cb” (i.e. a ‘blue’ chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (HSYNC+ODDEV) by up to 3 clock cycles to cope with different data/sync phasings, using configuration bits “Syncin_ad” (Reg. 4).

The STV0118 is thus fully slaved to the HSYNC signal, which means that lines may contain more or less samples than typical 525/625 system requirement.

If the digital line is shorter than its nominal value: the sample counter is re-initialized when the ‘early’ HSYNC arrives and all internal synchronization signals are re-initialized.

If the digital line is longer than its nominal value : the sample counter is stopped when it reaches its nominal end-of-line value and waits for the ‘late’ HSYNC before reinitializing.

The field counter is incremented on each ODDEV transition. The line counter is reset on the HSYNC following each active edge of ODDEV.

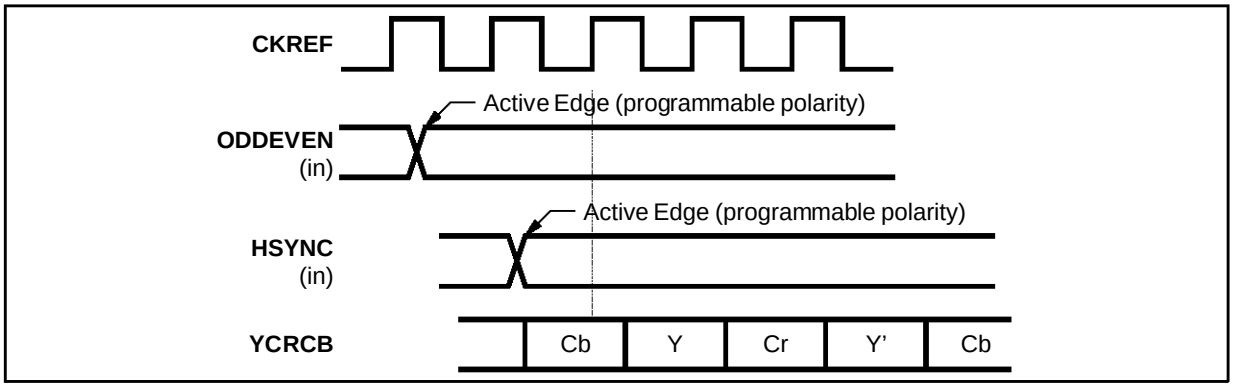
IV.5.1.2 - HSYNC+VSYNC Based Synchronization

Synchronization is performed on a line-by-line basis by locking onto incoming VSYNC and HSYNC signals. Refer to Figure 12 for waveforms and timings. The polarities of HSYNC and VSYNC are programmable and independent.

The incoming VSYNC signal is immediately transformed into a waveform identical to the odd/even waveform of an ODDEV signal, therefore the behavior of the core is identical to that described above for ODDEV+HSYNC based synchronization. Again, the phase relationship between HSYNC and the incoming YCrCb data is normally such that the first clock rising edge following the HSYNC active edge samples “Cb” (i.e. a ‘blue’ chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (HSYNC+VSYNC) by up to 3 clock cycles to cope with different data/sync phasings, using configuration bits “Syncin_ad” (Reg. 4).

The field counter is incremented on each active edge of VSYNC.

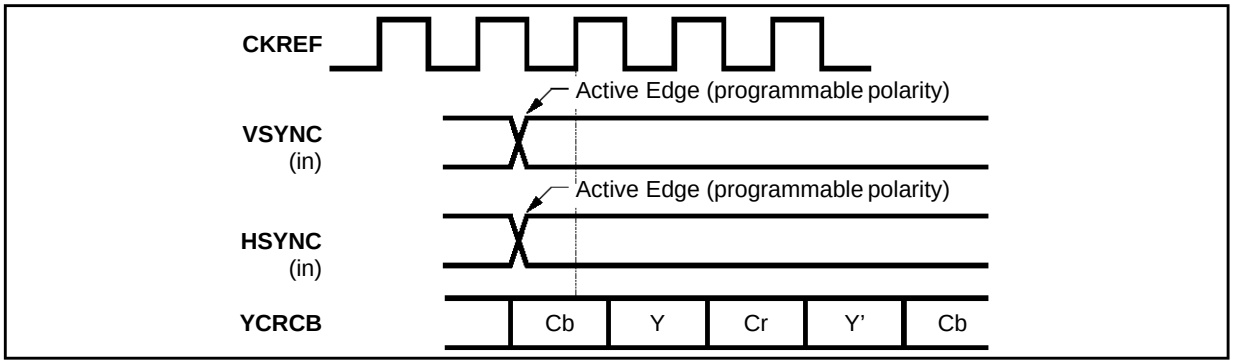
Figure 11 : HSYNC + ODDEVEN Based Slave Mode Sync Signals



Note : 1. This figure is valid for bits “syncin_ad[1:0]” = default.

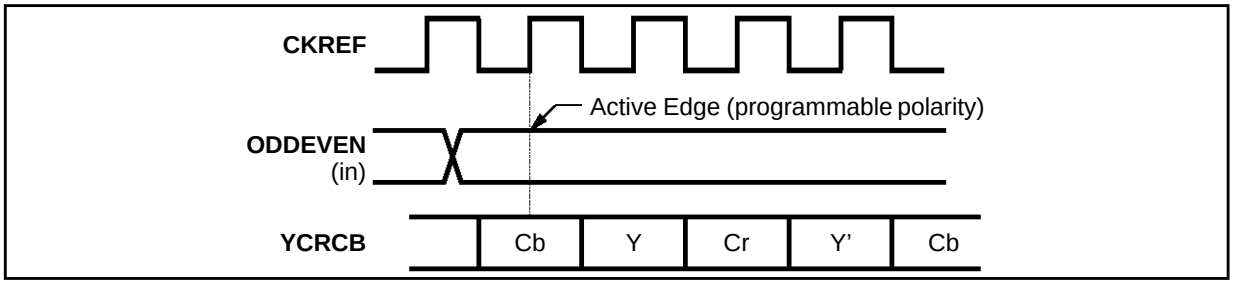
IV - FUNCTIONAL DESCRIPTION (continued)

Figure 12 : HSYNC + VSYNC Based Slave Mode Sync Signals



Notes : 1. This figure is valid for bits "syncin_ad[1:0]" = default.
2. The active edges of HSYNC and VSYNC should normally be simultaneous. It is permissible that HSYNC transitions before VSYNC, but VSYNC must not transition before HSYNC.

Figure 13 : ODDEVEN Based Slave Mode Sync Signals



Note : 1. This figure is valid for bits "syncin_ad[1:0]" = default.

IV.5.2 - Synchronization onto a Frame Sync Signal

IV.5.2.1 - ODDEV-only Based Synchronization

Synchronization is performed on a frame-by-frame basis by locking onto an incoming ODDEV signal. A line sync signal is derived internally and is also output as HSYNC. Refer to Figure 13 for waveforms and timings. The phase relationship between ODDEV and the incoming YCrCB data is normally such that the first clock rising edge following the ODDEV active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming ODDEV signal by up to 3 clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4).

The first active edge of ODDEV triggers generation of the analog sync signals and encoding of the incoming video data. Frames being supposed to be of constant duration, the next ODDEV active transition is expected at a precise time after the last ODDEV detected.

So, once an active ODDEV edge has been detected, checks that the following ODDEV are present at the expected instants are performed.

Encoding and analog sync generation carry on unless three successive fails of these checks occur.

In that case, three behaviors are possible, according to the configuration programmed (Reg. 1-2) :

- if 'free-run' is enabled, the STV0118 carries on outputting the digital line sync HSYNC and generating analog video just as though the expected ODDEV edge had been present. However, it will re-synchronize onto the next ODDEV active edge detected, whatever its location.
- if 'free-run' is disabled but bit 'sync_ok' is set in configuration register1, the STV0118 sets the active portion of the TV line to black level but carries on outputting the analog sync tips (on Ys and CVBS) and the digital line sync signal HSYNC.
- if 'free-run' is disabled and the bit 'sync_ok' is not set, all analog video is at black level and neither analog sync tips nor digital line sync are output.

Note that this mode is a frame-based sync mode, as opposed to a field-based sync mode, that is, only one type of edge (rising or falling, according to bit 'polv'in Reg 0) is of interest to the STV0118, the other one is ignored.

IV - FUNCTIONAL DESCRIPTION (continued)

IV.5.2.2 - VSYNC only Based Synchronization

Synchronization is performed on a frame-by-frame basis by locking onto an incoming VSYNC signal. An auxiliary line sync signal HSYNC must also be fed to the STV0118, which uses it to reconstruct from VSYNC and HSYNC information an internal odd/even waveform identical to that of an ODD-EVEN signal. Therefore the behavior of the core is identical to that described above for ODDEVEN only based synchronization (except that nothing is output on HSYNC pin since it is an input port in that mode). Note that HSYNC is an input but has no other use than allowing the STV0118 to decide whether an incoming VSYNC pulse flags an odd or an even field. In other words, the STV0118 does not lock onto HSYNC in this mode since this is NOT a line-locked mode.

The phase relationship between VSYNC and the incoming YCrCb data is normally such that the first clock rising edge following the VSYNC active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (VSYNC+HSYNC) by up to 3 clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4).

IV.5.3 - Synchronization onto Data-embedded Sync Words

IV.5.3.1 - 'End-of-frame' Word Based Synchronization

Synchronization is performed by extracting the 1-to-0 transitions of the 'F' flag (end-of-frame) from the 'EAV' (End-of-Active Video) sequence embedded within ITU-R656 / D1 compliant digital video streams. Both a frame sync signal and a line sync signal are derived and are made available externally as ODDEVEN and HSYNC (see Figure 14).

The first successful detection of the 'F' flag triggers generation of the analog sync signals and encoding of the incoming video data. Frames being supposed to be of constant duration, the next EAV word containing the 'F' flag is expected at a precise time after the latest detection.

So, once an active 'F' flag has been detected, checks that the following flags are present within the incoming video stream at the expected times are performed.

Encoding and analog sync generation carry on unless three successive fails of these checks occur.

In that case, three behaviors are possible, according to the configuration programmed :

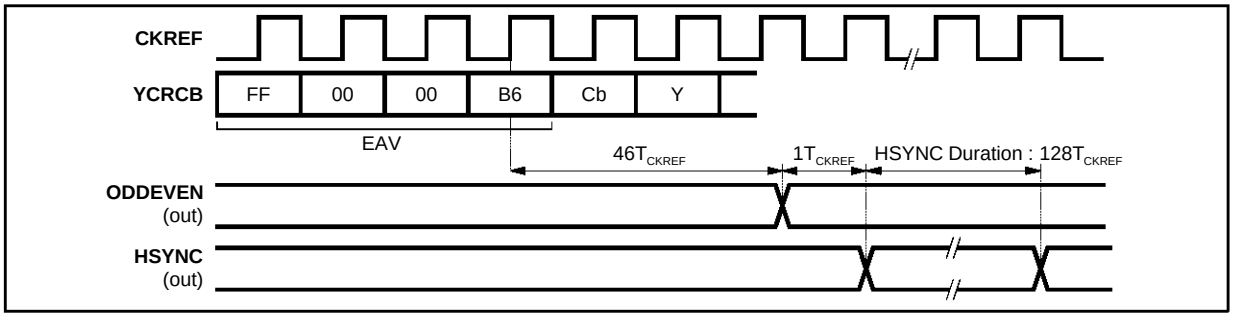
- if 'free-run' is enabled, the STV0118 carries on generating the digital frame and line syncs (ODD-EVEN and HSYNC) and generating analog video just as though the expected 'F' flag had been present. However, it will re-synchronize onto the next 'F' flag detected within the incoming CCIR656/D1 video stream.
- if 'free-run' is disabled but the bit 'sync_ok' is set in the configuration registers, the STV0118 sets the active portion of the TV line to black level but carries on outputting the analog sync tips (on Ys and CVBS) and the digital frame and line sync signals ODDEVEN and HSYNC.
- if 'free-run' is disabled and the bit 'sync_ok' is not set, all analog video is at black level and neither analog sync tips nor digital frame/line sync are output.

The SAV and EAV words are Hamming-decoded. After detection of two successive errors, a bit is set in the status register to inform the micro-controller of the poor transmission quality.

IV.5.3.2 - 'End-of-line' Word Based Synchronization

Synchronization is performed by extracting the 'F' and 'H' flags from the 'SAV' (Start of Active Video) and 'EAV' (End of Active Video) words embedded within ITU-R656/D1 compliant digital video streams. A line sync signal and a frame sync signal are derived internally from these flags and are output on the HSYNC and ODDEVEN/VSYNC pins in output mode. These signals are also exploited by the core of the circuit which treats them like it treats incoming ODDEVEN and HSYNC signals in HSYNC+ODDEV based synchronization (see Section IV.5.1.1).

Figure 14 : Data (EAV) Based Slave Mode Sync Signals



IV - FUNCTIONAL DESCRIPTION (continued)

IV.6 - Input Demultiplexer

The incoming 27Mbit/s YCrCb data is demultiplexed into a 'blue-difference' chroma information stream, a 'red-difference' chroma information stream and a luma information stream. Incoming data bits are treated as blue, red or luma samples according to their relative position with respect to the sync signals in use and to the content of configuration bits "Syncin_ad" (slave modes) or "Syncout_ad" (master mode).

The ITU-R601 recommendation defines the black luma level as Y = 16dec and the maximum white luma level as Y = 235dec. Similarly it defines 225 quantization levels for the color difference components (Cr, Cb), centered around 128.
Accordingly, incoming YCrCB samples can be saturated in the input multiplexer with the following rules :

- for Cr or Cb samples :
  Cr, Cb > 240 ⇒ Cr, Cb saturated at 240
  Cr,Cb < 16 ⇒ Cr, Cb saturated at 16
- for Y samples :
  Y > 235 ⇒ Y saturated at 235
  Y < 16 ⇒ Y saturated at 16

This avoids having to heavily saturate the composite video codes before digital-to-analog conversion in case erroneous or unrealistic YCrCb samples are input to the encoder (there may otherwise be overflow errors in the codes driving the DACs), and therefore avoids genera-ting a distorded output waveform.

However, in some applications, it may be desirable to let 'extreme' YCrCb codes pass through the demultiplexer. This is also possible, provided that bit "maxdyn" is set in configuation register 6.

In this case, only codes 00hex and FFhex are overridden: if such codes are found in the active video samples, they are forced to 01hex and FEhex.

In any case, the YCrCb codes are not overridden for EAV/SAV decoding

The demultiplexer is also able to handle 54Mbit/s YCrCb streams for dual encoding applications. Refer to Section IV.17, "Dual Encoding Application - 54Mbit/s YCrCB interface".

IV.7 - Sub-carrier Generation

A Direct Digital Frequency Synthesizer (DDFS) using a 24-bit phase accumulator, generates the required color sub-carrier frequency. This oscillator feeds a quadrature modulator which modulates the baseband chrominance components.

The sub-carrier frequency is obtained from the following equation :

$$Fsc = (24\text{-bit Increment Word} / 2^{24}) \times CKREF$$

Hard-wired Increment Word values are available for each standard (except for 'NTSC-4.43') and can be automatically selected. Alternatively (according to bit 'selrst' in Reg. 2.), the frequency can be fully customized by programming other values into a dedicated Increment Word Register (Reg. 10-11-12). This allows for instance to encode "NTSC-4.43" or "PAL-M-4.43".

This is done with the following procedure :

- Program the required increment in Registers 10 to 12
- Set bit 'selrst' to '1' in Configuration Register 2
- Perform a software reset (Reg. 6).
  Caution : this sets back all bits from Reg. 7 onwards to their default value, when they can be reset.

Warning : if a standard change occurs after the software reset, the increment value is automatically re-initialized with the hardwired or loaded value according to bit selrst.

The reset phase of the color sub-carrier can also be software-controlled (Reg. 13-14).

The sub-carrier phase can be periodically reset to its nominal value to compensate for any drift introduced by the finite accuracy of the calculations. Sub-carrier phase adjustment can be performed every line, every eight field, every four field, or every two field (Register 2 bits valrst[1:0]).

IV - FUNCTIONAL DESCRIPTION (continued)

IV.8 - Burst Insertion

The color reference burst is inserted so as to always start with a positive zero crossing of the subcarrier sine wave. The first and last half-cycles have a reduced amplitude so that the burst envelope starts and ends smoothly.

The burst contains 9 or 10 sine cycles of 4.43361875MHz or 3.579545MHz according to the standard programmed in the Control Register (Reg. 0, bits std[1:0]), as follows :

- NTSC-M	9 cycles of	3.579542MHz
- PAL-BDGHI	10 cycles of	4.43361875MHz
- PAL-M	9 cycles of	3.57561149MHz
- PAL-N	9 cycles of	3.5820558MHz

It is possible to turn the burst off (no burst insertion) by setting configuration bit 'bursten' to 0 (register2).

Notes : - Two strategies exist for burst insertion: one is to merely gate and shape the subcarrier for burst insertion, the other is more elaborated and is to always start the burst with a positive-going zero crossing. In the first case the phase of the subcarrier when the burst starts is not controlled, with the consequence that some of its first and last cycles are more heavily distorded. The second solution guarantees smooth start and end of burst with a maximum of undistorded burst cycles and can only be beneficial to chroma decoders, it is the solution implemented in the STV0118.

- While the first option gave constant burst start time but uncontrolled initial burst phase, the second solution guarantees start on a positive-going zero crossing with the consequence that two burst start locations are visible over successive lines, according to the line parity. This is normal and explained below.
- In NTSC, the relation between subcarrier frequency and line length creates a 180o subcarrier phase difference (with respect to the horizontal sync) from one line to the next according to the line parity. So if the burst always starts with the same phase (positive-going zero crossing), this means the burst will be inserted at time X or at time $X+T_{NTSC}/2$ after the horizontal sync tip according to the line parity, where T_{NTSC} is the duration of one cycle of the NTSC burst.
- With PAL, a similar rationale holds, and again there will be two possible burst start locations. The subcarrier phase difference (with respect to the horizontal sync) from one line to the next in that case is either 0 or 180o with the following series: A-A-B-B-A-A-…-etc. where A denotes 'A-type' bursts and B denotes 'B-type' bursts, A-type and B-type being 180° out of phase with respect to the horizontal sync. So 2 locations are possible, one for A-type, the other for B-type (see Figure 8).
- This assumes a periodic reset of the subcarrier is automatically performed (see bits valrst[1:0] in Reg 2). Otherwise, over several frames, the start of burst will drift within an interval of one a subcarrier's cycle. THIS IS NORMAL and means the burst is correctly locked to the colors encoded. The equivalent effect with a gated burst approach would be the following : the start location would be fixed but the phase with which the burst starts (with respect to the horizontal sync) would be drifting.

IV.9 - Luminance Encoding

The demultiplexed Y samples are band-limited and interpolated at CKREF clock rate. The resulting luminance signal is properly scaled before insertion of any Closed-captions, CGMS or Teletext data and synchronization pulses.

The interpolation filter compensates for the sin(x)/ x attenuation inherent to D/A conversion and greatly simplifies the output stage filter (refer to Figures 15 to 17 for characteristic curves).

Figure 15 : Luma Filtering Including DAC Attenuation

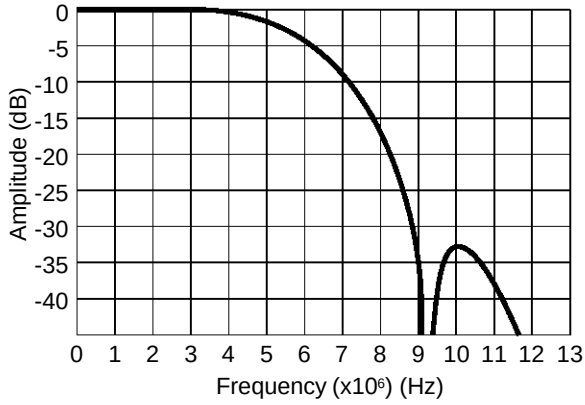


Figure 16 : Luma Filtering with 3.58MHz Trap, Including DAC Attenuation

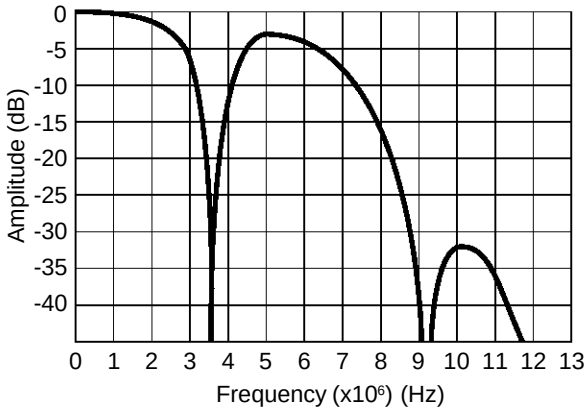
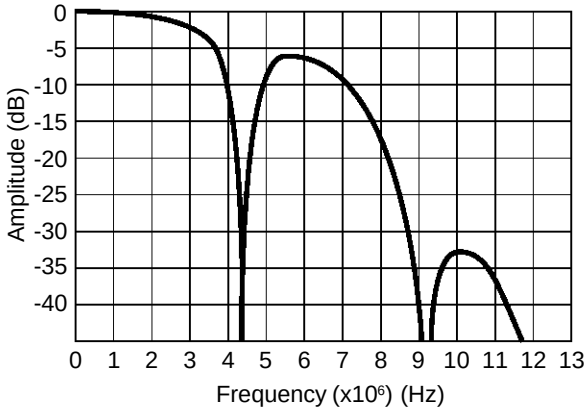


Figure 17 : Luma Filtering with 4.43MHz Trap, Including DAC Attenuation



IV - FUNCTIONAL DESCRIPTION (continued)

In addition, the luminance that is added to the chrominance to create the composite CVBS signal can be trap-filtered at 3.58MHz (NTSC) or 4.43MHz (PAL). This allows to cope with application oriented towards low-end TV sets which are subject to cross-color if the digital source has a wide luminance bandwidth (e.g. some DVD sources). Note that the trap filter does not affect the S-VHS luminance output nor the RGB outputs.
A 7.5 IRE pedestal can be programmed if needed with all standards (see Reg1, bit setup). This allows in particular to encode Argentinian and non-Argentinian PAL-N, or Japanese NTSC (NTSC with no set-up).
A programmable delay can be inserted on the luminance path to compensate any chroma/luma delay introduced by off-chip filtering (chroma and luma transitions being coincident at the DAC output with default delay) (Reg3, bits del[2:0]).

IV.10 - Chrominance Encoding

U and V chroma components are computed from demultiplexed Cb, Cr samples. Before modulating the subcarrier, these are band-limited and interpolated at CKREF clock rate. This processing eases the filtering following D/A conversion and allows a more accurate encoding. A set of 4 different filters is available for chroma filtering to fit a wide variety of applications in the different standards and include filters recommended by ITU-R Rec624-4 and SMPTE170-M. The available 3dB bandwidths are 1.1, 1.3, 1.6 or 1.9MHz, refer to Figures 18 to 22 for the various frequency responses (Reg1, bits flt[1:0]).
The narrower bandwidths are useful against cross-luminance artefacts, the wider bandwidths allow to keep higher chroma contents and then an improved image quality.

IV.11 - Composite Video Signal Generation

The composite video signal is created by adding the luminance (after optional trap filtering, Reg 3 bits entrap and trap_pal) and the chrominance components. A saturation function is included in the adder to avoid overflow errors should extreme luminance levels be modulated with highly saturated colors (this does not correspond to natural colors but may be generated by computers or graphic engines).
A 'color killing' function is available (Reg 1, bit coki) whereby the composite signal contains no chrominance, i.e. replicates the trap-filtered luminance. Note that this function does not suppress the chrominance on the S-VHS outputs (nevertheless suppressing the S-VHS chrominance is possible using bit "bkg_c" in Reg 5).

Figure 18 : Various Chroma Filters Available + RGB Filter

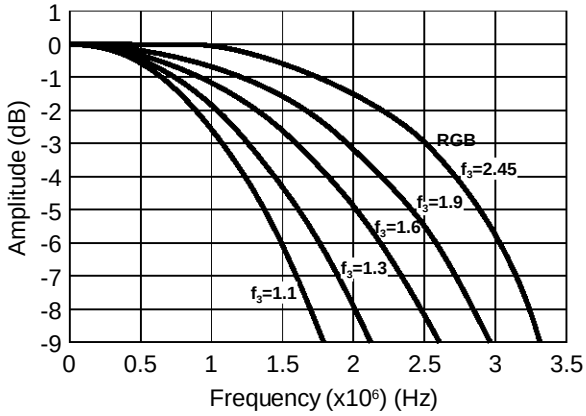


Figure 19 : 1.1MHz Chroma Filter (flt = 00)

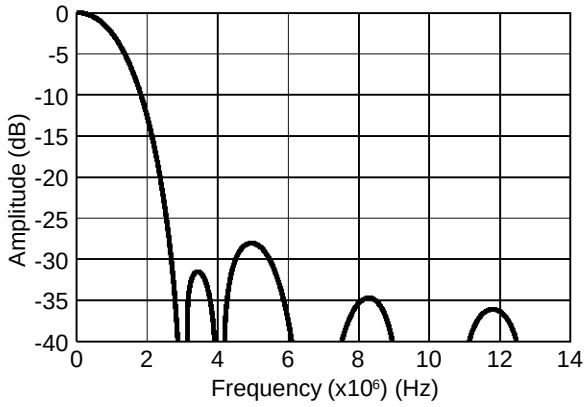
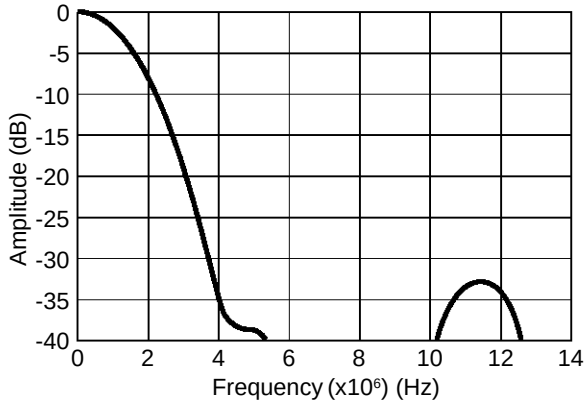


Figure 20 : 1.3MHz Chroma Filter (flt = 01)



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 21 : 1.6MHz Chroma Filter (flt = 10)

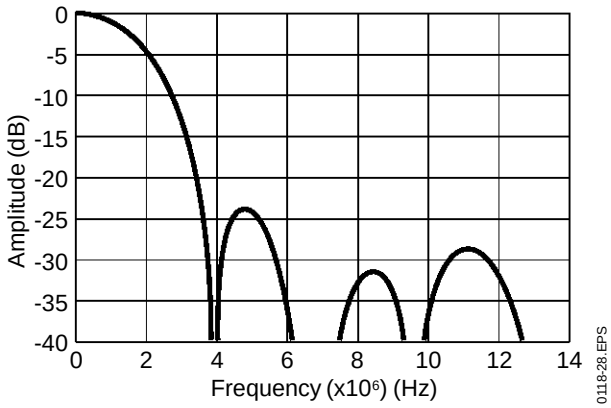
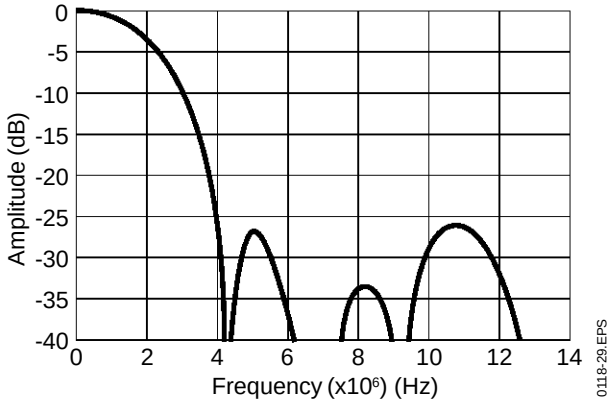


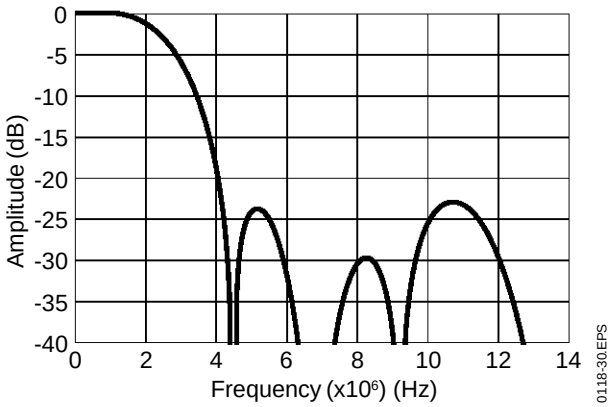
Figure 22 : 1.9MHz Chroma Filter (flt = 11)



IV.12 - RGB Encoding

After demultiplexing, the Cr and Cb samples feed a 4 times interpolation filter. The resulting baseband chroma signal has a 2.45MHz bandwidth (Figure 23) and is combined with the filtered luma component to generate R, G, B samples at 27MHz.

Figure 23 : RGB Chroma Filtering



IV.13 - Closed Captioning

Closed-captions (or data from an Extended Data Service as defined by the Closed-Captions specification) can be encoded by the circuit. The closed caption data is delivered to the circuit through the I^2C interface. Two dedicated pairs of bytes (two bytes per field), each pair preceded by a clock run-in and a start bit can be encoded and inserted on the luminance path on a selected TV line. The Clock Run-In and Start code are generated by the STV0118.

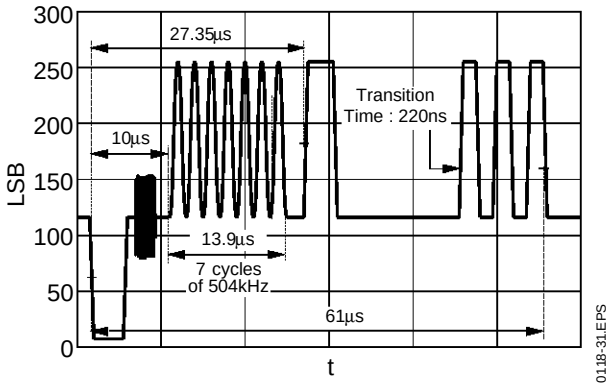
Closed-caption data registers are double-buffered so that loading can be performed anytime, even during line 21/284 or any other selected line.

User register 39 (resp. 41) contains the first byte to send (LSB first) after the start bit on the appropriate TV line in field 1 (resp. field 2), and user register 40 (resp. 42) contains the second byte to send. The TV line number where data is to be encoded is programmble (Reg. 37, 38). Lines that may be selected include those used by the StarSight data broadcast system. Closed-captions data has priority over CGMS programmed for the same line.

The internal Clock Run-In generator is based on a Direct Digital Frequency Synthesizer. The nominal instantaneous data rate is 503.5kbit/s(i.e. 32 times the NTSC line rate). Data LOW corresponds nominally to 0 IRE, data HIGH corresponds to 50 IRE at the DAC outputs. Refer to Figure 24.

When closed-captioning is on (bits cc1/cc2 in Reg.1), the CPU should load the relevant registers (reg. 39 and 40, or 41 and 42) once every frame at most (although there is in fact some margin due to the double-buffering). Two bits are set in the status register in case of attempts to load the closed-caption data registers too frequently, these can be used to regulate loading rate.

Figure 24 : Example Closed-caption Waveform



IV - FUNCTIONAL DESCRIPTION (continued)

The closed caption encoder considers that closed caption data has been loaded and is valid on completion of the write operation into register 40 for field1, into register 42 for field 2. If closed caption encoding has been enabled and no new data bytes have been written into the closed caption data registers when the closed caption window starts on the appropriate TV line, then the circuit outputs two US-ASCII NULL characters with odd parity after the start bit.

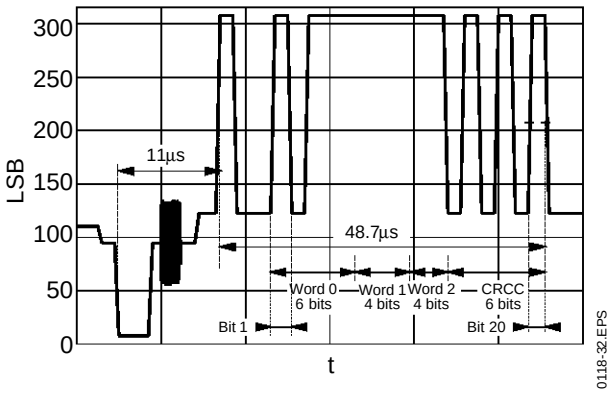
IV.14 - CGMS Encoding

CGMS (Copy Generation Management System - also known as VBID and described by standard CPX-1204 of EIAJ) data can be encoded by the circuit. Three bytes (20 significant bits) are delivered to the chip via the I2C interface. Two reference bits ('1' then '0') are encoded first, followed by 20 bits of CGMS data (including a Cyclic Redundancy Check sequence, not computed by the device and supplied to it as part of the 20 data bits). The reference bits are generated locally by the STV0118. Refer to Figure 25 for a typical CGMS waveform.

When CGMS encoding is enabled, the CGMS (see bit encgms in Reg 3) waveform is continously present once in each field, on lines 20 and 283 (SMPTE-525 line numbering).

The CGMS data register is double-buffered, which means that it can be loaded anytime (even during line 20/283) without any risk of corrupting CGMS data that could be in the process of being encoded. The CGMS encoder considers that new CGMS data has been loaded and is valid on completion of the write operation into register 33

Figure 25 : Example CGMS Waveform



IV.15 - Teletext Encoding

The STV0118 is able to encode Teletext according to the "CCIR/ITU-R Broadcast Teletext System B" specification, also known as "World System Teletext".

In DVB applications, Teletext data is embedded within DVB streams as MPEG data packets. It is the responsibility of a "Transport Layer Processing" IC (or demultiplexer), like SGS-Thomson's ST20-based "TP2", to sort out incoming data packets and in particular to store Teletext packet in a buffer, which then passes them to the STV0118 on request.

IV.15.1 - Signals Exchanged

The STV0118 and the Teletext buffer exchange 2 signals: TTXS (Teletext Synchronization) going from the STV0118 to the Teletext Buffer and TTXD (Teletext Data) going from the Teletext Buffer to the STV0118.

The TTXS signal is a request signal generated on selected lines. In response to this signal, the Teletext buffer is expected to send 360 Teletext bits to the STV0118 for insertion of a Teletext line into the analog video signal.

The duration of the TTXS window is 1402 reference clock periods (51.926µs), which corresponds to the duration of 360 Teletext bits (see Transmission Protocol below).

Following the TTXS rising edge the encoder expects data from the Teletext buffer after a programmable number (2 to 9) of 27MHz master clock periods. Data is transmitted synchronously with the master clock at an average rate of 6.9375Mbit/s according to the protocol described below. It consists, in order of transmission, of 16 Clock Run-In bits, 8 Framing Code bits and the 336 bits (42 bytes) that represent one Teletext packet.

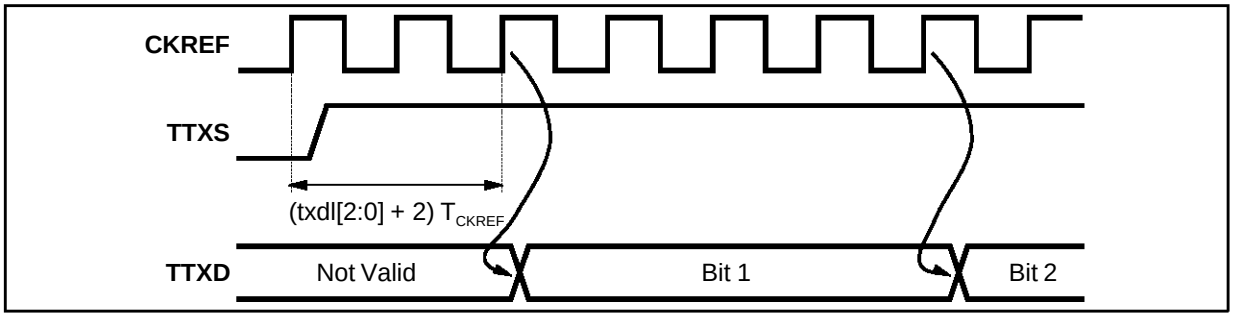
IV.15.2 - Transmission Protocol

In order to transmit the Teletext data bits at an average rate of 6.9375Mbit/s, which is about 1/3.89 times the master clock frequency, the following scheme is adopted :

The 360-bit packet is regarded as nine 37-bit sequences plus one 27-bit sequence. In every sequence, each Teletext data bit is transmitted as a succession of 4 identical samples at 27 Msample/s, except for the 10th, 19th, 28th and 37th bits of the sequence which are transmitted as a succession of 3 identical samples. This protocol is compatible with SGS-Thomson's ST-20 based Tranport Layer IC ("TP2").

IV - FUNCTIONAL DESCRIPTION (continued)

Figure 26 : "TTXS Rising" to "First Valid Sample" Delay for txdl[2:0] = 0



IV.15.3 - Programming

IV.15.3.1 - 'TTXS Rising' to 'First Valid Sample' Delay Programming

The encoder expects the Teletext buffer to clock out the first Teletext data sample on the (2+N)th rising edge of the master clock following the rising edge of TTXS (Figure 26 depicts this graphically for N=0). 'N' is programmable from 0 to 7 (i.e. overall delay is programmable from TWO to NINE 27MHz cycles) via 3 dedicated bits located in the Configuration Register4 : "txdl[2:0]".

IV.15.3.2 - Teletext Line Selection

Five dedicated registers allow to program Teletext encoding in various areas of the Vertical Blanking Interval (VBI) of each field. A total of 4 such areas (i.e. blocks of contiguous Teletext lines) can independently be defined within the two VBIs of one frame (e.g. 2 blocks in each VBI, or 3 blocks in field1 VBI and one in field2 VBI, etc.). Further, under certain circumstances, it is possible to define up to 4 areas in each VBI.

Programming is performed using 4 "Teletext Block Definition" registers (TTXBD1, TTXBD2, TTXBD3,TTXBD4) and a "Teletext Block Mapping" register (TTXBM). Refer to the description of user registers 34 to 38 for details.

IV.15.4 - Teletext Pulse Shape

The shape and amplitude of a single Teletext pulse are depicted in Figure 27, its relative power spectral density is given in Figures 28 and 29 and is substantially zero at frequencies above 5MHz, as required by the World System Teletext specification.

Figure 27 : Shape and Amplitude of a Single Teletext Symbol

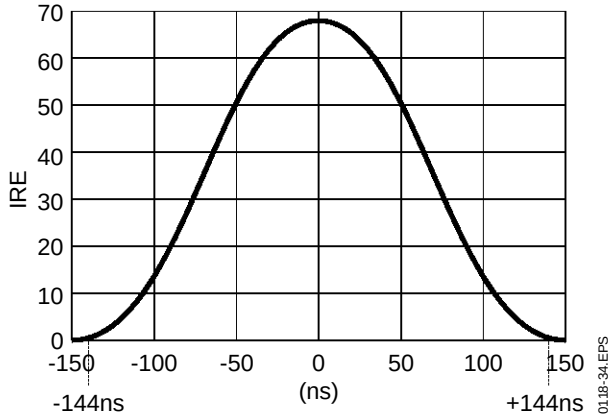
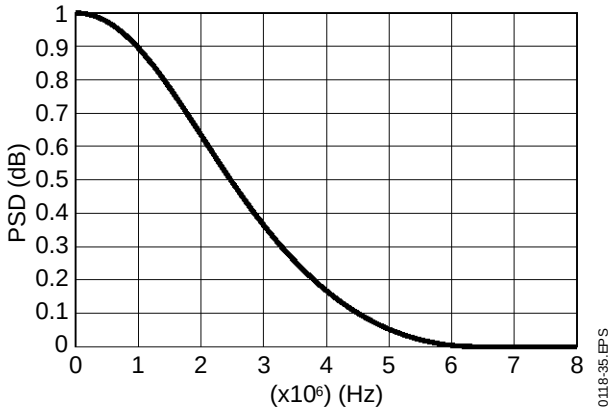
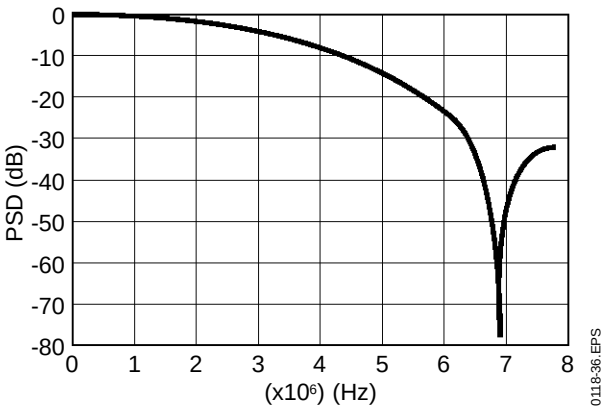


Figure 28 : Linear PSD Scale



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 29 : Logarithmic PSD Scale



IV.16 - I²C Bus

An external micro-controller controls the STV0118 via an I²C bus by writing into or reading from internal registers. The I²C interface supports the "fast I²C protocol" (up to 400kHz - and potentially more).

The default I²C addresses of the STV0118 are :
- in write mode : "01000000" (40 hex)
- in read mode : "01000001" (41 hex)

After a hardware reset, it is these addresses that the STV0118 recognizes.

It is possible to modify the default I²C address by tiing the TTXS/CSI2C pin to logic '1' and validating the change by writing into a dedicated bit in Register 6.

In that case, the STV0118 has a new I²C address :
- in write mode : "01000010" (42 hex)
- in read mode : "01000011" (43 hex)

Once the I²C address has been changed, it cannot be modifed anymore until the next hardware reset.

Note that these I²C addresses are the same as those used by the STV0117/STV0117A/STV0119 (others SGS-THOMSON PAL/NTSC Digital Encoder).

It is expected that I²C address changes will normally be needed for dual encoding applications. The exact procedure to change the I²C addresses is detailed below, in the section that deals with dual encoding applications.

Write and read operations are described in Figures 30 and 31.

Figure 30 : I²C Write Operation (default address at power-on, CSI2C ≠ '1')

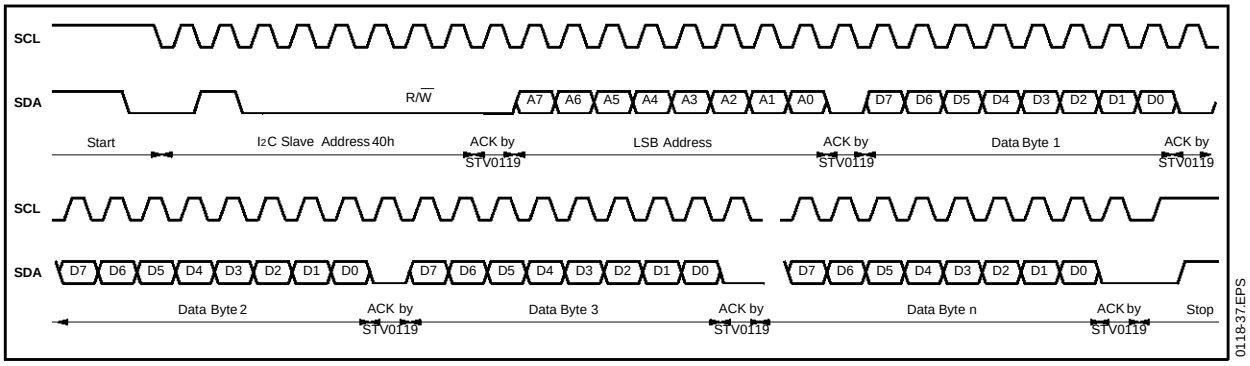
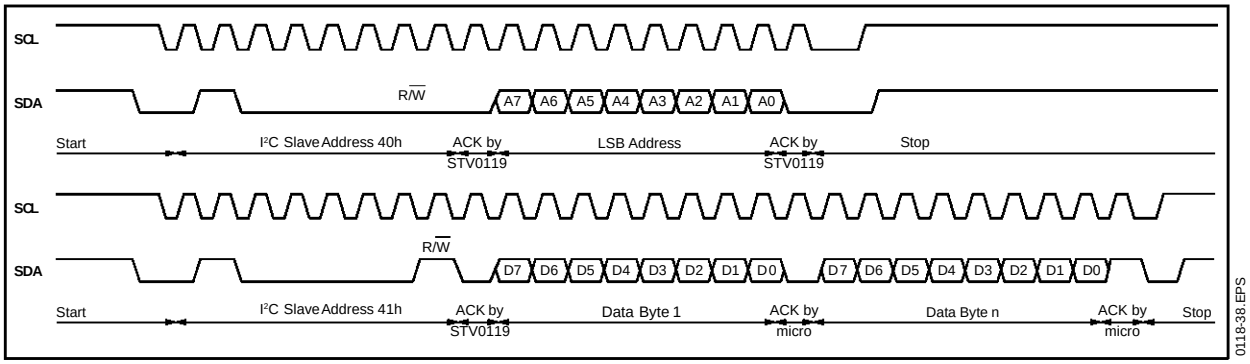


Figure 31 : I²C Read Operation (default address at power-on, CSI2C ≠ '1')



IV - FUNCTIONAL DESCRIPTION (continued)

IV.17 - Dual Encoding Application with 54Mbit/s YCrCb Interface

The STV0118 is able to interface with SGS-THOMSON's MPEG decoders capable of supplying a 54-Mbit/s YCrCB multiplex, like the STi3520M. This multiplex embeds two 27Mbit/s YCrCb video streams, one with OSD contents and the other without OSD content (see Figure 32). Note that the frequency of the reference clock supplied to the encoder is still 27MHz, only both edges are used in the interface.

The MPEG decoder being usually slaved to the encoder, if two encoders are to be used in parallel, one of them must be master and the other must be slave. Figure 33 shows a typical dual encoding application (although other applications where two STV0118's are slave are possible).

It is also necessary to be able to control independently the encoders. One solution is to have two separate I^2C busses (one for each encoder) running from the microcontroller (this is possible on SGS-THOMSON's ST20, which features two I^2C busses), another solution is to change the I^2C chip address of one of the STV0118.

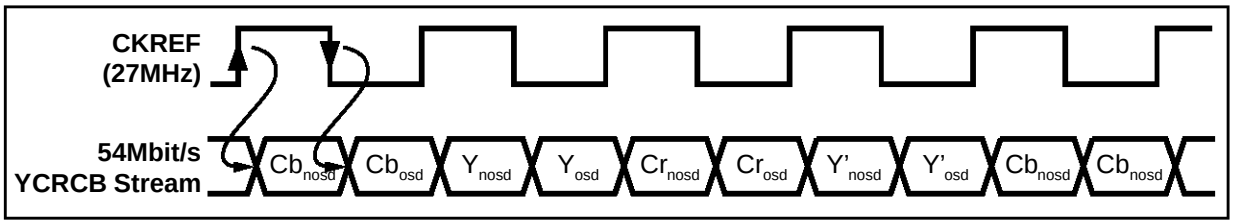
This can be done with the following procedure :

- If no Teletext is required, tie pin TTXS/ CSI2C of the 1st encoder to '0'.
- If Teletext encoding is needed, connect the TTXS/CSI2C pin of the first encoder to both the TTXS input pin of the Teletext Buffer / Transport IC (e.g. SGS-Thomson's TP2) and a pull-down resistor (needed for power-on configuration).
- Connect TTXS/CSI2C of the second encoder to logic '1'.
- Before performing any Teletext-related programming, set to '1' bit "chgi2c" in configuration register 6.

On hardware reset, both encoders have the same default I^2C address (40-41hex). When bit "chgi2c" toggles to '1', the I^2C address of the first encoder (with TTXS/CSI2C pulled low) keeps unchanged at 40-41hex, whilst the I^2C address of the second encoder (with TTXS/CSI2C = '1') switches to 42-43hex and can no more be changed until the next hardware reset.

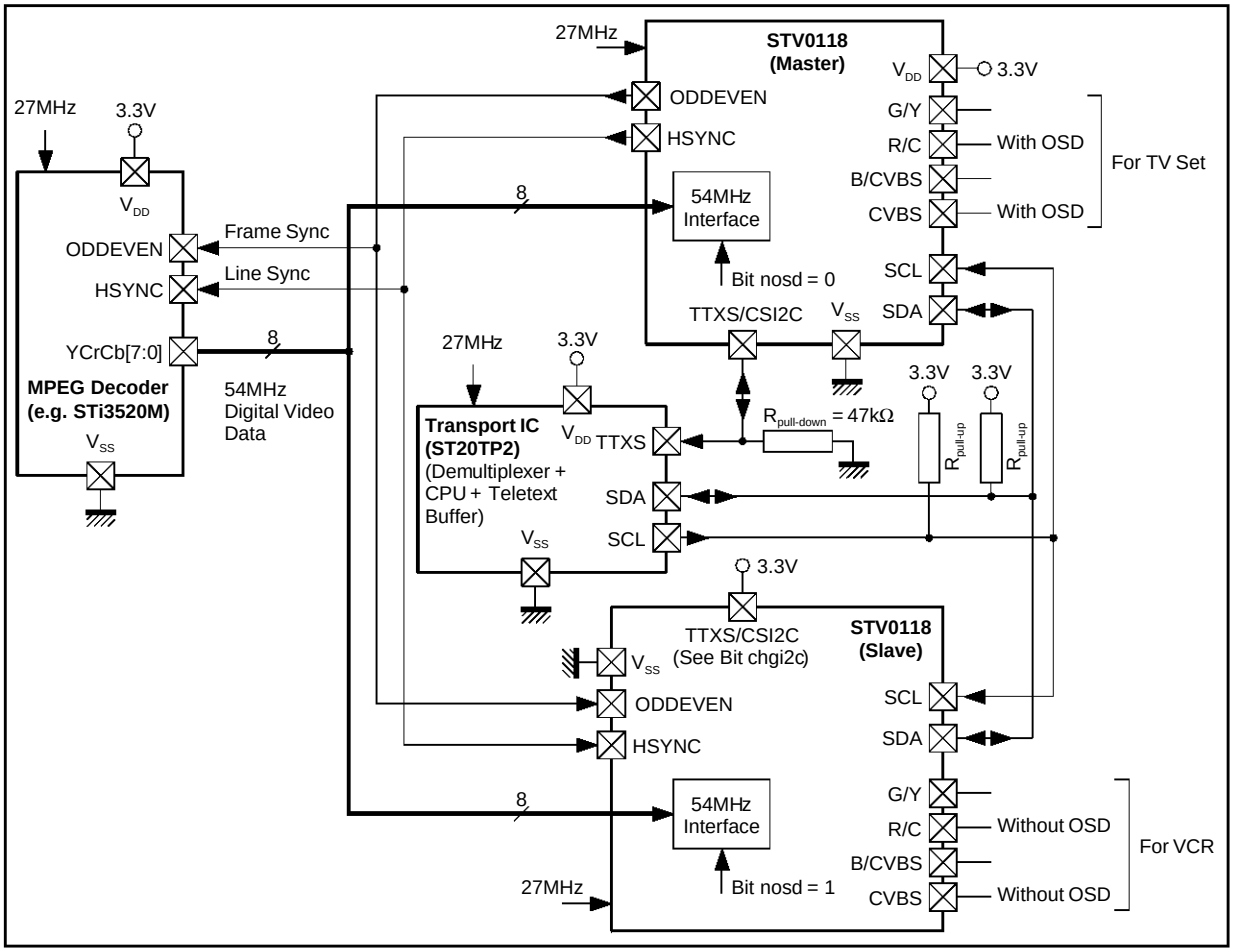
After I^2C address change, the second encoder must be programmed to choose the YCRCb incoming data stream on the falling edge of CKREF (see bit 'nosd' in configuration register 3).

Figure 32 : 54Mbit/s Dual YCRCB Stream



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 33 : Typical Dual Encoding Application



IV - FUNCTIONAL DESCRIPTION (continued)

IV.18 - Line Skip / Line Insert Capability

This patented feature of the STV0118 offers the possibility to cut the cost of the application by suppressing the need for a VCXO.

Ideally, the master clock used on the application board and fed to the MPEG decoding IC would have exactly same frequency as the clock that was used when the MPEG data was encoded. Obviously this is not realistic; up to now a solution commonly chosen is to dynamically adjust the clock on the board as close to the 'ideal' clock as possible with the help of time stamps embedded within the MPEG stream. Such a kind of tracking often involves the use of a VCXO : when the MPEG data buffer fills up to more than some threshold the clock frequency is increased, when it empties down to some other threshold the clock frequency is lowered.

The STV0118 offers an alternative, cost-saving solution: by programming the two bits jump and dec_ninc in configuration Reg6, the STV0118 is able to reduce or increase the length of some frames in a way that will not introduce visible artefacts (even if comb-filtering is used). These bits should be set according to the level of the MPEG data buffer. Refer to Section VI.2 Register 6, Register 9 and Registers 21-22-23 for complete bit description.

Operation with the STV0118 as sync master is as follows :

- If the MPEG data buffers fills up too much: set bit "jump" to '1' and bit "dec_ninc" to '1'.The STV0118 will reduce the length of the current frame (Bit "jump" will then automatically be reset to '0').
- If the MPEG data buffers empties too much: set bit "jump" to '1' and bit "dec_ninc" to '0'.The STV0118 will increase the length of the current frame (Bit "jump" will then automatically be reset to '0').

These operations can be repeated until the MPEG data buffer is inside its fixed limits.

It is also possible to use the line skip/repeat capability in non-interlaced mode.

This functionality of the STV0118 is also available in slave mode, in this case the sync signals supplied to the STV0118 must be in accordance with the modified frame lengthes programmed.

IV.19 - CVBS, S-VHS and RGB Analog Outputs

Four out of six video signals (composite CVBS, S-VHS (Y/C) and RGB) can be directed to 4 analog output pins through 9-bit D/A converters operating at the reference clock frequency.
The available combinations (see bit 'rgb_nyc' in Reg5) are :
S-VHS (Y/C) + CVBS + CVBS1
or : R, G, B + CVBS1.

A single external analog power supply pair is used for all DACs, but two independent pairs of current and voltage references are needed. Each current reference pin is normally connected externally to a resistor tied to the analogue ground, whilst each voltage reference pin is normally connected to a capacitance tied to the analogue ground.

The internal current sources are independent from the positive supply, thanks to a bangap, and the consumption of the DACs is constant whatever the codes converted.

Any unused DAC may be independently disabled by software, in which case its output is at 'neutral' level (blanking for luma and composite outputs, no color for chroma output, black for RGB outputs). For applications where a single CVBS output is required, the RGB/CVBS+S-VHS Triple DAC should be disabled and Pins $I_{REF(RGB)}$, VR_RGB tied to analog power supply.

V - CHARACTERISTICS

V.1 - Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DDx}	DC Supply Voltage	-0.3, 4.0	V
V_{IN}	Digital Input Voltage	-0.3, V_{DD} + 0.3	V
V_{OUT}	Digital Output Voltage	-0.3, V_{DD} + 0.3	V
I_{REF}	Analog Input Reference Current	2	mA
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-40, +150	°C
P_{tot}	Total Power Dissipation	500	mW

V.2 - Thermal Data

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	DC Junction-Ambient Thermal Resistance with sample soldered on a PCB	Typ.	76	°C/W

V.3 - DC Electrical Characteristics

T_{amb} = 25°C/70°C, V_{DDA} = V_{DD} = 3.3V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{DDA}	Analog Positive Supply Voltage		3.0	3.3	3.6	V
V_{DD}	Digital Supply Voltage		3.0	3.3	3.6	V
I_{DDA}	Analog Current Consumption	RI_{REF} =1.2kΩ, R_L = 200Ω, C_L = 50pF, CKREF = 27MHz, V_{DD} = 3.6V autotest mode, static input signals	20		50	mA
I_{DD}	Digital Current Consumption		20	35	50	mA
DIGITAL INPUTS						
V_{IL}	Input Voltage	Low level (any other pins)			0.8	V
V_{IH}	Input Voltage SCL and SDA Except SCL and SDA	High level (any other pins)	 2.0 2.0		 4.5 V_{DD}	V
I_L	Input Leakage Current Input Pins (see note 2) Bi-directional Pins	V_{IL} min or V_{IH} max	 -10 -10		 80 10	 µA µA
C_{IN}	Input Capacitance Input Pins Bi-directional Pins			 0.1 5		 pF pF
SDA OUTPUT						
V_L	Output Voltage	Low level, I_O = 2mA			0.4	V
DIGITAL OUTPUT						
V_{OH}	Output Voltage	High level (I_{OH} = -4mA)	2			V
V_{OL}	Output Voltage	Low level (I_{OL} = 4mA)			0.6	V
D/A CONVERTER						
RI_{REF}	Resistance for reference Current Source for 3 D/A Converters	I_{REF} = V_{REF}/RI_{REF}, V_{REF} = 1.12V typ.		1.2		kΩ
V_O	Output Voltage Dyn	RI_{REF} = 1.2kΩ, R_L = 200Ω (Max. code - Min. Code)	0.95		1.10	V_{PP}
	DAC to DAC V_O max code (tri-DAC only)	RI_{REF} = 1.2kΩ, R_L = 200Ω			3	%
ILE	LF Integral Non-linearity	RI_{REF} = 1.2kΩ, R_L = 200Ω		± 1		LSB
DLE	LF Differential Non-linearity	RI_{REF} = 1.2kΩ, R_L = 200Ω		± 0.5		LSB

Notes : 1. This product withstands 1.4kV (The MIL883C Norm requires 2.0kV).
This product withstands 150V (The EIAJ Norm requires 200V).
2. The high value for input Pins is due to internal pull-down resistance.

V - CHARACTERISTICS (continued)

V.4 - AC Electrical Characteristics

T_{amb} = 25°C/70°C, V_{DDA} = V_{DD} = 3.3V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INPUT (YCRCB[7:0], HSYNC, VSYNC/ODDEVEN)						
tsu	Input Data Set-up Time	CKREF rising edge, CKREF = 27MHz	6			ns
tho	Input Data Hold Time	CKREF rising edge, CKREF = 27MHz	3			ns
ACTIVE PERIOD FOR NRESET						
tRSTL	Input Low Time		200			ns
REFERENCE CLOCK : CKREF						
1/tC_REF	Clock Frequency			27		MHz
tD_REF	Clock Duty Cycle		35*		65*	%
tR_REF	Clock Rise Time				5	ns
tF_REF	Clock Fall Time				5	ns
I^2C CLOCK : SCL						
tC_SCL	Clock Cycle Time	Rpull_up = 4.7kΩ			2	MHz
tD_SCL	Clock Duty Cycle			50		%
tL_SCL	LOW Level Cycle	Rpull_up = 4.7kΩ	250			ns
DIGITAL OUTPUTS						
td_HSYNC	Delay Time	CKREF rising edge CKREF = 27MHz, C_L = 50pF			10	ns
td_ODDEVEN	Delay Time	CKREF rising edge CKREF = 27MHz, C_L = 50pF			10	ns

* In case of double encoding these values must be compatible with the ycrcb transmitter.

VI - REGISTERS

VI.1 - Register Mapping

configuration0	R/W	00	std1	std0	sync2	sync1	sync0	polh	polv	freerun
configuration1	R/W	01	blkli	flt1	flt0	sync_ok	coki	setup	cc2	cc1
configuration2	R/W	02	nintrl	enrst	bursten	xxx	selrst	rstosc	valrst1	valrst0
configuration3	R/W	03	entrap	trap_pal	encgms	nosd	del2	del1	del0	xxx
configuration4	R/W	04	syncin _ad1	syncin _ad0	syncout _ad1	syncout _ad0	aline	txdl2	txdl1	txdl0
configuration5	R/W	05	rgb_nyc	bkcvbs1	reserved	reserved	bk_ys	bk_c	bk_cvbs	dacinv
configuration6	R/W	06	softreset	jump	dec_ninc	free_jump	xxx	xxx	chgi2c	maxdyn
reserved	xxx	07	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
reserved	xxx	08	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
status	R	09	hok	atfr	b2_free	b1_free	fieldct2	fieldct1	fieldct0	jumping
increment_dfs	R/W	10	d23	d22	d21	d20	d19	d18	d17	d16
increment_dfs	R/W	11	d15	d14	d13	d12	d11	d10	d9	d8
increment_dfs	R/W	12	d7	d6	d5	d4	d3	d2	d1	d0
phase_dfs	R/W	13	-	-	-	-	-	-	o23	o22
phase_dfs	R/W	14	o21	o20	o19	o18	o17	o16	o15	o14
reserved	xxx	15	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
reserved	xxx	16	xxx	xxx	xxx	xxx	xxx	xxx	S	xxx
chipid	R	17	0	1	1	1	0	1	1	1
revid	R	18	0	0	0	0	0	0	0	1
reserved	R/W	19	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
reserved	R/W	20	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
line_reg	R/W	21	ltarg8	ltarg7	ltarg6	ltarg5	ltarg4	ltarg3	ltarg2	ltarg1
line_reg	R/W	22	ltarg0	lref8	lref7	lref6	lref5	lref4	lref3	lref2
line_reg	R/W	23	lref1	lref0	-	-	-	-	-	-
cgms_bit_1-4	R/W	31	-	-	-	-	bit1	bit2	bit3	bit4
cgms_bit_5-12	R/W	32	bit5	bit6	bit7	bit8	bit9	bit10	bit11	bit12
cgms_bit_13-20	R/W	33	bit13	bit14	bit15	bit16	bit17	bit18	bit19	bit20
ttx_block_1_def.	R/W	34	ttxbs1.3	ttxbs1.2	ttxbs1.1	ttxbs1.0	ttxbe1.3	ttxbe1.2	ttxbe1.1	ttxbe1.0
ttx_block_2_def.	R/W	35	ttxbs2.3	ttxbs2.2	ttxbs2.1	ttxbs2.0	ttxbe2.3	ttxbe2.2	ttxbe2.1	ttxbe2.0
ttx_block_3_def.	R/W	36	ttxbs3.3	ttxbs3.2	ttxbs3.1	ttxbs3.0	ttxbe3.3	ttxbe3.2	ttxbe3.1	ttxbe3.0
ttx_block_4_def.	R/W	37	ttxbs4.3	ttxbs4.2	ttxbs4.1	ttxbs4.0	ttxbe4.3	ttxbe4.2	ttxbe4.1	ttxbe4.0
ttx_block_map	R/W	38	ttxbmf1.1	ttxbmf1.2	ttxbmf1.3	ttxbmf1.4	ttxbmf2.1	ttxbmf2.2	ttxbmf2.3	ttxbmf2.4
c.c.c.F1	R/W	39	opc11	c117	c116	c115	c114	c113	c112	c111
c.c.c.F1	R/W	40	opc12	c127	c126	c125	c124	c123	c122	c121
c.c.c.F2	R/W	41	opc21	c217	c216	c215	c214	c213	c212	c211
c.c.c.F2	R/W	42	opc22	c227	c226	c225	c224	c223	c222	c221
cclif1	R/W	43	xxx	xxx	xxx	l1_4	l1_3	l1_2	l1_1	l1_0
cclif2	R/W	44	xxx	xxx	xxx	l2_4	l2_3	l2_2	l2_1	l2_0
reserved	xxx	45	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
...	...	...	...	...	...	...	...	...	...	...
reserved	xxx	63	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx

VI - REGISTERS (continued)

VI.2 - Register Contents and Description

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_0 - Configuration0

	MSB							LSB
Content	std1	std0	sync2	sync1	sync0	polh	polv	freerun
Default	1	0	0	1	0	0	1	0

std[1:0]

	std1	std0	Standard Selected
	0	0	PAL BDGHI
	0	1	PAL N (see bit set-up)
(*)	1	0	NTSC M
	1	1	PAL M

Note 1 : Standard on hardware reset is NTSC; any standard modification selects automatically the right parameters for correct subcarrier generation.

sync[2:0]

	sync2	sync1	sync0	Configuration (refer to Functional Description, Sections IV.4 and IV.5)
	0	0	0	ODDEVEN based SLAVE mode (frame locked)
	0	0	1	F only based SLAVE mode (frame locked)
(*)	0	1	0	ODDEV+HSYNC based SLAVE mode (line locked)
	0	1	1	'F'+'H' based SLAVE mode (line locked)
	1	0	0	VSYNC-only based SLAVE mode (frame locked) (see Note)
	1	0	1	VSYNC+HSYNC based SLAVE mode (line locked)
	1	1	0	MASTER mode
	1	1	1	AUTOTEST mode (color bar pattern)

Caution : In VSYNC-only based slave mode (sync[2:0]="100"), HSYNC is nevertheless needed as an input. Refer to Functional Description, Section IV.5.2.2.

polh Synchro : active edge of HSYNC selection (when input) or polarity of HSYNC (when output)

(*) 0 HSYNC is a negative pulse (128 T_{CKREF} wide) or falling edge is active

1 HSYNC is a positive pulse (128 T_{CKREF} wide) or rising edge is active

polv Synchro : active edge of ODDEVEN/VSYNC selection (when input) or polarity of ODDEV (when output) - See Note 2

0 Falling edge of ODDEVEN flags start of field1 (odd field) or VSYNC is active low

(*) 1 Rising edge of ODDEVEN flags start of field1 (odd field) or VSYNC is active high

Note 2 : In master mode : polarity of ODDEVEN output.
In slave by F (from EAV) : polv = 0 (cf D1 encoding) and ODDEVEN polarity is the image of F extracted from EAV words.

freerun Refer to Functional Description, Section IV.5

(*) 0 disabled

1 Enabled

Caution : This bit is taken into account in ODDEV-only, VSYNC-only or 'F' based slave modes and is irrelevant to other synchronization modes.

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_1 - Configuration1

	MSB							LSB
Content	blkli	flt1	flt0	sync_ok	coki	setup	cc2	cc1
Default	0	1	0	0	0	1	0	0

blkli Vertical Blanking Interval selection for active video lines area (refer to Functional Description, Section IV.2 and Figures 2 to 7).

(*) 0 ('partial blanking') Only following lines inside Vertical Interval are blanked
NTSC-M : lines [1..9], [263(half)..272] (525-SMPTE)
PAL-M : lines [523..6], [260(half)..269] (525-CCIR)
other PAL : lines [623(half)..5], [311..318] (625-CCIR)
This mode allows preservation of VBI data embedded within incoming YCrCb, e.g. Teletext (lines [7..22] and [320..335]), Wide Screen signalling (full line 23), Video Programing Service (line16), etc.).

1 ('full blanking') All lines inside VBI are blanked
NTSC-M : lines [1..19], [263(half)..282] (525-SMPTE)
PAL-M : lines [523..16], [260(half)..279] (525-CCIR)
other PAL : lines [623(half)..22], [311..335] (625-CCIR)

Note : blkli must be set to '0' when closed captions and are to be encoded on following lines :
- in 525/60 system: before line 20(SMPTE) or before line 283(SMPTE)
- in 625/50 system: before line 23(CCIR) or before line 336(CCIR)
For CGMS and Teletext encodings, blkli value is not taken into account.

flt[1:0] U/V Chroma filter bandwidth selection
(Refer to Functional Description, Section IV.10 and Figures 4 and 5)

	flt1	**flt0**	**3dB Bandwidth**	**Typical Application**
	0	0	f-3 = 1.1MHz	Low definition NTSC filter
	0	1	f-3 = 1.3MHz	Low definition PAL filter
(*)	1	0	f-3 = 1.6MHz	High definition NTSC filter (ATSC compliant) & PAL M/N (ITU-R 624.4 compliant)
	1	1	f-3 = 1.9MHz	High definition PAL filter: Rec 624 - 4 for PAL BDG/I compliant

sync_ok Availability of sync signals (analog and digital) in case of input synchronization loss with no free-run active (i.e. freerun=0) (Refer to Functional Description, Section IV.5)

(*) 0 No synchro output signals

1 Output synchros available on YS, CVBS and, when applicable, HSYNC (if output port), ODDEVEN (if output port), i.e same behavior as free-run except that video outputs are blanked in the active portion of the line

Caution : This bit is taken into account in ODDEV-only, VSYNC-only or 'F' based slave modes and is irrelevant to other synchronization modes.

coki Color killer (Refer to Functional Description, Section IV.11)

(*) 0 Color ON

1 Color suppressed on CVBS (and CVBS1) output signal (CVBS=YS) but color still present on C and RGB outputs. For color suppression on chroma DAC 'C', see register 5 bit bkg_c.

setup Pedestal enable (Refer to Functional Description, Section IV.9)

0 Blanking level and black level are identical on all lines
(ex : Argentinian PAL-N, Japan NTSC-M, PAL-BDGHI)

(*) 1 Black level is 7.5 IRE above blanking level on all lines outside VBI
(ex :Paraguayan and Uruguayan PAL-N)

In all standards, gain factor is adjusted to obtain the required levels for chrominance.

cc2, cc1 Closed caption encoding mode (Refer to Functional Description, Section IV.13)

	cc2	**cc1**	**Encoding Mode**
(*)	0	0	No closed caption/extended data encoding
	0	1	Closed caption/extended data encoding enabled in field 1 (odd)
	1	0	Closed caption/extended data encoding enabled in field 2 (even)
	1	1	Closed caption/extended data encoding enabled in both fields

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_2 - Configuration2

	MSB							LSB
Content	nintrl	enrst	bursten	xxxx	selrst	rstosc	valrst1	valrst0
Default	0	0	1	0	0	0	0	0

Refer to Functional Description, Section IV.7.

nintrl Non-interlaced mode select (Refer to Figures 3, 5 and 7)

(*) 0 Interlaced mode (625/50 or 525/60 system)

1 Non-interlaced mode(2x312/50 or 2x262/60 system)

Note : 'nintrl' update is internally taken into account on beginning of next frame.

enrst Cyclic update of DDFS phase

(*) 0 No cyclic subcarrier phase reset

1 Cyclic subcarrier phase reset depending of valrst1 and valrst0 (see below)

bursten Chrominance burst control

0 Burst is turned off on CVBS (and CVBS1), C and RGB outputs are not affected

(*) 1 Burst is enabled

selrst Selects set of reset values for Direct Digital Frequency Synthesizer

(*) 0 Hardware reset values for phase and increment of subcarrier oscillator (see description of registers 10 to 14 for values)

1 I^2C loaded reset values selected (see contents of Registers 10 to 14)

rstosc Software phase reset of DDFS (Direct Digital Frequency Synthesizer)

(*) 0 inactive

1 a 0-to-1 transition resets the phase of the subcarrier to either the hard-wired default phase value or the value loaded in Register 13-14 (according to bit 'selrst')

Note : Bit 'rstosc' is automatically set back to '0' after the oscillator reset has been performed.

valrst[1:0] Note : valrst[1:0] is taken into account only if bit 'enrst' is set

	valrst1	**valrst0**	**Selection**
(*)	0	0	Automatic reset of the oscillator every line
	0	1	Automatic reset of the oscillator every 2nd field
	1	0	Automatic reset of the oscillator every 4th field
	1	1	Automatic reset of the oscillator every 8th field

Resetting the oscillator means here forcing the value of the accumulator phase to its nominal value to avoid accumulating errors due to the finite number of bits used internally. The value to which the accumulator is reset is either the hard-wired default phase value or the value loaded in Register 13-14 (according to bit 'selrst'), to which a 0°, 90°, 180°, or 270° correction is applied according to the field and line on which the reset is performed.

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_3 - Configuration3

	MSB							LSB
Content	entrap	trap_pal	encgms	nosd	del2	del1	del0	xxx
Default	0	0	0	0	0	0	0	0

entrap Enable trap filter

(*) 0 Trap filter disabled

1 Trap filter enabled

trap_pal Refer to Functional Description, Section IV.9

Note : 'trap_pal' is taken into account only if bit 'entrap' is set.

(*) 0 To select the NTSC trap filter (centered around 3.58MHz) (see Figure 16)

1 To select the PAL trap filter (centered around 4.43MHz) (see Figure 17)

encgms CGMS encoding enable (Refer to Functional Description, Section IV.14)

(*) 0 Disabled

1 Enabled

Note : When encgms is set to 1 Closed-Captions/Extended Data Services should not be programmed on lines 20 and 283 (525/60, SMPTE line number convention).

nosd Choice of active edge of 'ckref' (master clock) that samples incoming YCrCb data (Refer to Functional Description, Section IV.17).

(*) 0 'ckref' rising edge (e.g. data with OSD coming from STi3520M)

1 'ckref' falling edge (e.g. data without OSD coming from STi3520M)

Note : Typically, this bit is used when two STV0118's are used in a 'dual encoding' configuration.

del[2:0] Delay on luma path with reference to chroma path
(Refer to Functional Description, Section IV.9)

	del2	**del1**	**del0**	**Delay on luma path with reference to chroma path** (one pixel corresponds to 1/13.5MHz (74.04ns))
	0	1	0	+ 2 pixel delay on luma
	0	0	1	+ 1 pixel delay on luma
(*)	0	0	0	+ 0 pixel delay on luma
	1	1	1	- 1 pixel delay on luma
	1	1	0	- 2 pixel delay on luma
	Other			+ 0 pixel delay on luma

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_4 - Configuration4

	MSB							LSB
Content	syncin_ad1	syncin_ad0	syncout_ad1	syncout_ad0	aline	txdl2	txdl1	txdl0
Default	0	0	0	0	0	0	0	0

syncin_ad Adjustment of incoming sync signals (Refer to Functional Description, Section IV.5). Used to insure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is slaved to incoming sync signals (incl. 'F/H' flags stripped off ITU-R656/D1 data).

	syncin_ad1	**syncin_ad0**	**Internal delay undergone by incoming sync**
(*)	0	0	Nominal
	0	1	+1 ckref
	1	0	+2 ckref
	1	1	+3 ckref

syncout_ad Adjustment of outgoing sync signals (Refer to Functional Description, Section IV.4). Used to insure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is master and supplies sync signals.

	syncout_ad1	**syncout_ad0**	**Delay added to sync signals before they are output**
(*)	0	0	Nominal
	0	1	+1 ckref
	1	0	+2 ckref
	1	1	+3 ckref

aline Video active line duration control (Refer to Functional Description, Section IV.2)

(*) 0 Full digital video line encoding (720 pixels - 1440 clock cycles)

1 Active line duration follows ITU-R/SMPTE 'analog' standard requirements

txdl[2:0] Teletext data latency (* "000" default) (Refer to Functional Description, Section IV.15) The encoder will clock in the first Teletext data sample on the $(2+txdl[2:0])^{th}$ rising edge of the master clock following the rising edge of TTXS (Teletext Synchro signal, supplied by the encoder).

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_5 - Configuration5

	MSB							LSB
Content	rgb_nyc	bkcvbs1	reserved	reserved	bk_ys	bk_c	bk_cvbs	dacinv
Default	0	0	1	1	0	0	0	0

rgb_nyc Selection between RGB or S-VHS/CVBS outputs present on DACs (refer to Functional Description, Section IV.12)

(*) 0 Y - C - CVBS - CVBS1 on DACs

1 R - G - B - CVBS1 on DACs

bkcvbs1 Blanking of DAC CVBS

(*) 0 DAC CVBS in normal operation

1 DAC input code forced to blanking level

bk_ys Blanking of DAC G/Y'

(*) 0 DAC G/Y in normal operation

1 DAC input code forced to black level (if G) or blanking level (if Y)

bk_c Blanking of DAC 'R/C'

(*) 0 DAC R/C in normal operation

1 DAC input code forced to black level (if R) or neutral level [no color] (if C)

bk_cvbs Blanking of DAC 'B/CVBS'

(*) 0 DAC B/CVBS in normal operation

1 DAC input code forced to black level (if B) or blanking level (if CVBS)

dacinv 'Inverts' DAC codes to compensate for an inverting output stage in the application

(*) 0 DAC non inverted inputs

1 DAC inverted inputs

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_6 - Configuration6

	MSB							LSB
Content	softreset	jump	dec_ninc	free_jump	xxxx	xxxx	chgi2c	maxdyn
Default	0	0	0	1	0	0	0	0

softreset Software reset

(*) 0 No reset

1 Software reset

Note : Bit 'softreset' is automatically reset after internal reset generation.
Software reset is active during 4 CKREF periods. When softreset is activated, all the device is reset as with hardware reset except for the first six user registers (configurations) and for registers 10 up to 14 (increment and phase of oscillator), 31-33, 34-37 and 39-42.

jump, dec_ninc, free_jump

jump	dec_ninc	free_jump	
0	0	0	Normal mode (no line skip/insert capability) CCIR : 313/312 or 263/262 non-interlaced : 312/312 or 262/262
0	x	1	Manual mode for line insert ("dec_ninc" = 0) or skip ("dec_ninc" = 1) capability. Both fields of all the frames following the I^2C writing are modified according to "Iref" and "Itarg" bits of registers 21-22-23 (by default, "Iref" = 0 and "Itarg" = 1 which leads to normal mode above).
1	0	0	Automatic line insert mode. The 2^{nd} field of the frame following the I^2C writing is increased. Line insertion is done after line 245 in 525/60 and after line 330 in 625/50. "Iref" and "Itarg" bits are ignored.
1	1	0	Automatic line skip mode. The 2^{nd} field of the frame following the I^2C writting is decreased. Line suppression is done after line 245 in 525/60 and after line 330 in 625/50. "Iref" and "Itarg" bits are ignored.
1	x	1	Not be used

Notes :
- Refer to Functional Description (Section IV.18)
- bit "jump" is automatically reset after use.

chgi2c Chip address selection

(*) 0 Chip address : write = 40hex ; read = 41hex

1 Chip address : write = 42hex; read = 43hex

Note : Setting this bit to 1 changes the chip address provided that pin ttxs/csi2c is tied to Vdd when the 0-to-1 transition occurs. Refer to sections IV.16 and IV.17. The new address is valid until the next hardware reset.

maxdyn Max dynamic magnitude allowed on YCrCb inputs for encoding
(Refer to Functional Description, Section IV.6).

(*) 0 10hex to EBhex for Y, 10hex to E0hex for chrominance (Cr,Cb)

1 01hex to FEhex for Y, Cr and Cb

Note : In any case, EAV and SAV words are replaced by blanking values before being fed to the luminance and chrominace processings

REGISTER_7 and 8 : *Reserved*

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_9 - Status *(read only)*

	MSB							LSB
Content	hok	atfr	buf2_free	buf1_free	fieldct2	fieldct1	fieldct0	jumping

hok Hamming decoding of frame sync flag embedded within ITU-R656/D1 compliant YCrCb streams.
0 Consecutive errors
(*) 1 A single or no error
Note : signal quality detector is issued from Hamming decoding of EAV,SAV from YCrCb

atfr Frame synchronization flag (slave mode only)
(*) 0 Encoder not synchronized
1 Encoder synchronized

buf2_free Closed caption registers access condition for field 2
(refer to Functional Description, Section IV.13)
Closed caption data for field 2 is buffered before being output on the relevant TV line; buf2_free is reset if the buffer is temporarily unavailable. If the microcontroller can guarantee that registers 41 and 42 (cccf2) are never written more than once between two frame reference signals, then bit 'buf2_free' will always be true (set). Otherwise, closed caption field2 registers access might be temporarily forbidden by resetting bit 'buf2_free' until the next field2 closed caption line occurs.
Note that this bit is false (reset) when 2 pairs of data bytes are awaiting to be encoded, and is set back immediately after one of these pairs has been encoded (so at that time,encoding of the last pair of bytes is still pending)
(*) Reset value = 1 (access authorized)

buf1_free Closed caption registers access condition for field 1
Same as buf2_free but concerns field 1.
(*) Reset value = 1 (access authorized)

fieldct[2:0] Digital field identification number
000 Indicates field 1
...
111 Indicates field 8
fieldct[0] also represents the odd/even information (odd='0', even='1')

jumping Indicates whether a frame length modification has been programmed at '1' from programming of bit 'jump' to end of frame(s) concerned.
(*) Default = 0
Refer to register 6 and registers 21-22-23.

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTERS_10_11_12- Increment_dfs : *Increment for digital frequency synthesizer*

	MSB							LSB
register_10	d23	d22	d21	d20	d19	d18	d17	d16
register_11	d15	d14	d13	d12	d11	d10	d9	d8
register_12	d7	d6	d5	d4	d3	d2	d1	d0

These registers contain the 24-bit increment used by the DDFS if bit 'selrst' equals '1' to generate the frequency of the subcarrier i.e. the address that is supplied to the sine ROM. It therefore allows to customize the subcarrier frequency synthesized. Refer to Functional Description, Section IV.7.

1 LSB ~ 1.6 Hz

The procedure to validate usage of these registers instead of the hard-wired values is the following :
- Load the registers with the required value
- Set bit 'selrst' to 1 (Reg 2)
- Perform a software reset (Reg 6)

Notes : The values loaded in Reg10-11-12 are taken into account after a software reset, and ONLY IF bit 'selrst'='1' (Reg. 2)

These registers are never reset and must be explicitly written into to contain sensible information. On hardware reset (=> 'selrst'=0) or on soft reset with selrst='0', the DDFS is initalized with a hardwired increment, independent of Registers 10-12. These hardwired values being out of any user register these cannot be read out of the STV0118.

These values are :

Value	**Frequency Synthesized**	**Ref.Clock**
d[23:0] : 21F07C hexa for NTSC M (*)	f = 3.5795452MHz	27MHz
d[23:0] : 2A098B hexa for PAL BGHIN	f = 4.43361875 MHz	27MHz
d[23:0] : 21F694 hexa for PAL N	f = 3.5820558MHz	27MHz
d[23:0] : 21E6F0 hexa for PAL M	f = 3.57561149MHz	27MHz

'NTSC-4.43' can be obtained with d[23:0] value like for PAL BGHI but with standard fixed as NTSC.

REGISTERS_13_14 - Phase_dfs : *Static phase offset for digital frequency synthesizer (10 bits only)*

	MSB							LSB
register_13	-	-	-	-	-	-	o23	o22
register_14	o21	o20	o19	o18	o17	o16	o15	o14

Under certain circumstances (detailed below), these registers contain the 10 MSBs of the value with which the phase accumulator of the DDFS is initialized after a 0-to-1 transition of bit 'rstosc' (Reg 2), or after a standard change, or when cyclic phase readjustment has been programmed (see bits valrst[1:0] of Reg 2). The 14 remaining LSBs loaded into the accumulator in these cases are all '0's (this allows to define the phase reset value with a 0.35° accuracy).

The procedure to validate usage of these registers instead of the hard-wired values is the following :
- Load the registers with the required value
- Set bit 'selrst' to 1 (Reg 2)
- Perform a software reset (Reg 6)

Notes : Registers 13-14 are never reset and must be explicitly written into to contain sensible information. If bit 'selrst'=0 (e.g. after a hardware reset) the phase offset used to reinitialize the DDFS is the hard-wired value. The hard-wired values being out of any register, they cannot be read out of the STV0118.

These are :
- D9C000hex for PAL BDGHI, N, M
- 1FC000hex for NTSC-M

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_15 : *Reserved*
REGISTER_16 : *Reserved*

REGISTER_17 : chipID *(read only) : STV0118 Identification Number*

0 1 1 1 0 1 1 0 (codes 118 in binary format)

REGISTER_18 : revID *(read only) : STV0118 Revision Number*

0 0 0 0 0 0 0 1 (for first revision)

REGISTER_19 : *Reserved*
REGISTER_20 : *Reserved*

REGISTERS_21_22_23: line_reg = ltarg[8:0] and lref[8:0]

	MSB							LSB
register_21	ltarg8	ltarg7	ltarg6	ltarg5	ltarg4	ltarg3	ltarg2	ltarg1
register_22	ltarg0	lref8	lref7	lref6	lref5	lref4	lref3	lref2
register_23	lref1	lref0	-	-	-	-	-	-

These registers may be used to jump from a reference line (end of that line) to the beginning of a target line of the SAME FIELD.

However, not all lines can be skipped or repeated with no problem and, if needed, this functionality has to BE USED WITH CAUTION.

lref[8:0] contains in binary format the reference line from which a jump is required. ltarg[8:0] contains the target line binary number.

Default values: lref[8:0] = 000000000 and ltarg[8:0] = 000000001

REGISTER_31-32-33 - cgms_bit[1:20] : CGMS Data registers *(20 bits only)*

	MSB							LSB
register_31	-	-	-	-	b1	b2	b3	b4
register_32	b5	b6	b7	b8	b9	b10	b11	b12
register_33	b13	b14	b15	b16	b17	b18	b19	b20

These registers are never reset.

Word0A => bit1....bit3
Word0B => bit4....bit6
Word1 => bit7....bit10
Word2 => bit11....bit14

CRC => bit15...bit20 (not internally computed)

Refer to Functional Description, Section IV.14

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_34-35-36-37 - ttx_block_[1:4]_def. : Teletext Block Definition

(Refer to Functional Description, Section IV.15)

	MSB							LSB
register_34 txbd1	txbs1.3	txbs1.2	txbs1.1	txbs1.0	txbe1.3	txbe1.2	txbe1.1	txbe1.0
register_35 txbd2	txbs2.3	txbs2.2	txbs2.1	txbs2.0	txbe2.3	txbe2.2	txbe2.1	txbe2.0
register_36 txbd3	txbs3.3	txbs3.2	txbs3.1	txbs3.0	txbe3.3	txbe3.2	txbe3.1	txbe3.0
register_37 txbd4	txbs4.3	txbs4.2	txbs4.1	txbs4.0	txbe4.3	txbe4.2	txbe4.1	txbe4.0

These are four Teletext Block Definition registers, used in conjunction with Reg 38 (Teletext Block Mapping). Each of these registers defines a start line (TXBSx[3:0]) and an end line (TXBEx[3:0]). [TXBSx = Teletext Block Start for block x, TXBEx = Teletext Block End for block x]

When applying to field1 : TXBSx[3:0]=0 codes line 7,
...
TXBSx[3:0]=i codes line 7+i,
...
TXBSx[3:0]=15dec ('1111'bin) codes line 7+15=22

When applying to field2 : TXBSx[3:0]=0 codes line 320,
...
TXBSx[3:0]=i codes line 320+i,
...
TXBSx[3:0]=15dec ('1111'bin) codes line 320+15=335

(ITU-R601/625 line numbering)

DEFAULT value: none, registers 34-37 are never reset.

REGISTER_38 - ttx_block_map : Teletext Block Mapping

	MSB							LSB
register_38	txmf1.1	txmf1.2	txmf1.3	txmf1.4	txmf2.1	txmf2.2	txmf2.3	txmf2.4

(txmf1 stands for 'Teletext Block Mapping to field1, txmf2 stands for 'Teletext Block Mapping to field2)

This register allows to map the blocks of Teletext lines defined by registers 34 to 37 to either field1, field2 or both :

Its default value is "00000000"

txmf1.N defines whether txbdN (Nth teletext block, see reg34-37 above) applies to field 1,

txmf2.N defines whether txbdN (Nth teletext block, see reg34-37 above) applies to field 2.

In other words, if txmf1.N=1 then Teletext will be encoded in field 1 from the line defined by txbsN.[3:0] (see above) to the line defined by txbeN.[3:0].

Similarly, if txmf2.N=1 then Teletext will be encoded in field 2 from the line defined txbsN.[3:0] (see above) to the line defined by txbeN.[3:0].

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_39-40 - cccf1 : Closed caption characters/extended data for field 1

First byte to encode in field1 :

	MSB							LSB
register_39	opc11	c117	c116	c115	c114	c113	c112	c111

opc11 Odd-parity bit of US-ASCII 7-bit character c11[7:1]

Second byte to encode in field1:

	MSB							LSB
register_40	opc12	c127	c126	c125	c124	c123	c122	c121

opc12 Odd-parity bit of US-ASCII 7-bit character c12[7:1]
Default value : none, but closed captions enabling without loading these registers will issue character NULL. Registers 39-40 are never reset.

REGISTER_41-42 : cccf2 : Closed caption characters/extended data for field 2

First byte to encode in filed2 :

	MSB							LSB
register_41	opc21	c217	c216	c215	c214	c213	c212	c211

opc21 Odd-parity bit of US-ASCII 7-bit character c21[7:1]

Second byte to encode in field2 :

	MSB							LSB
register_42	opc22	c227	c226	c225	c224	c223	c222	c221

opc22 Odd-parity bit of US-ASCII 7-bit character c22[7:1]
Default value : none but closed captions enabling without loading these registers will issue character NULL. Registers 41-42 are never reset.

REGISTER_43 - cclif1 : Closed caption/extended data line insertion for field 1

TV line number where closed caption/extended data is to be encoded in field 1 is programmable through the following register :

	MSB							LSB
register_43	xxxx	xxxx	xxxx	l1_4	l1_3	l1_2	l1_1	l1_0
Default	0	0	0	0	1	1	1	1

- 525/60 system : (525-SMPTE line number convention)
  Only lines 10 through 22 should be used for closed caption or extended data services (line 1 through 9 contain the vertical sync pulses with equalizing pulses).
  l1[4:0] = 00000 no line selected for closed caption encoding
  l1[4:0] = 000xx do not use these codes
  ...
  l1[4:0] = i code line (i+6) (SMPTE) selected for encoding
  ...
  l1[4:0] = 11111 line 37 (SMPTE) selected
- 625/50 system: (625-CCIR/ITU-R line number convention)
  Only lines 7 through 23 should be used for closed caption or extended data services.
  l1[4:0] = 00000 no line selected for closed caption encoding
  ...
  l1[4:0] = i code line (i+6) (CCIR) selected for encoding (i > 0)
  ...
  l1[4:0] = 11111 line 37 (CCIR) selected
  (*) Default value = 01111 line 21 (525/60, 525-SMPTE line number convention).
  This value also corresponds to line 21 in 625/50 system,(625-CCIR line number convention).

VI - REGISTERS (continued)

VI.2 - Register Contents and Description (continued)

(*) = DEFAULT mode when NRESET pin is active (LOW level)

REGISTER_44 - cclif2 : Closed caption/extended data line insertion for field 2

TV line number where closed caption/extended data is to be encoded in field 2 is programmable through the following register :

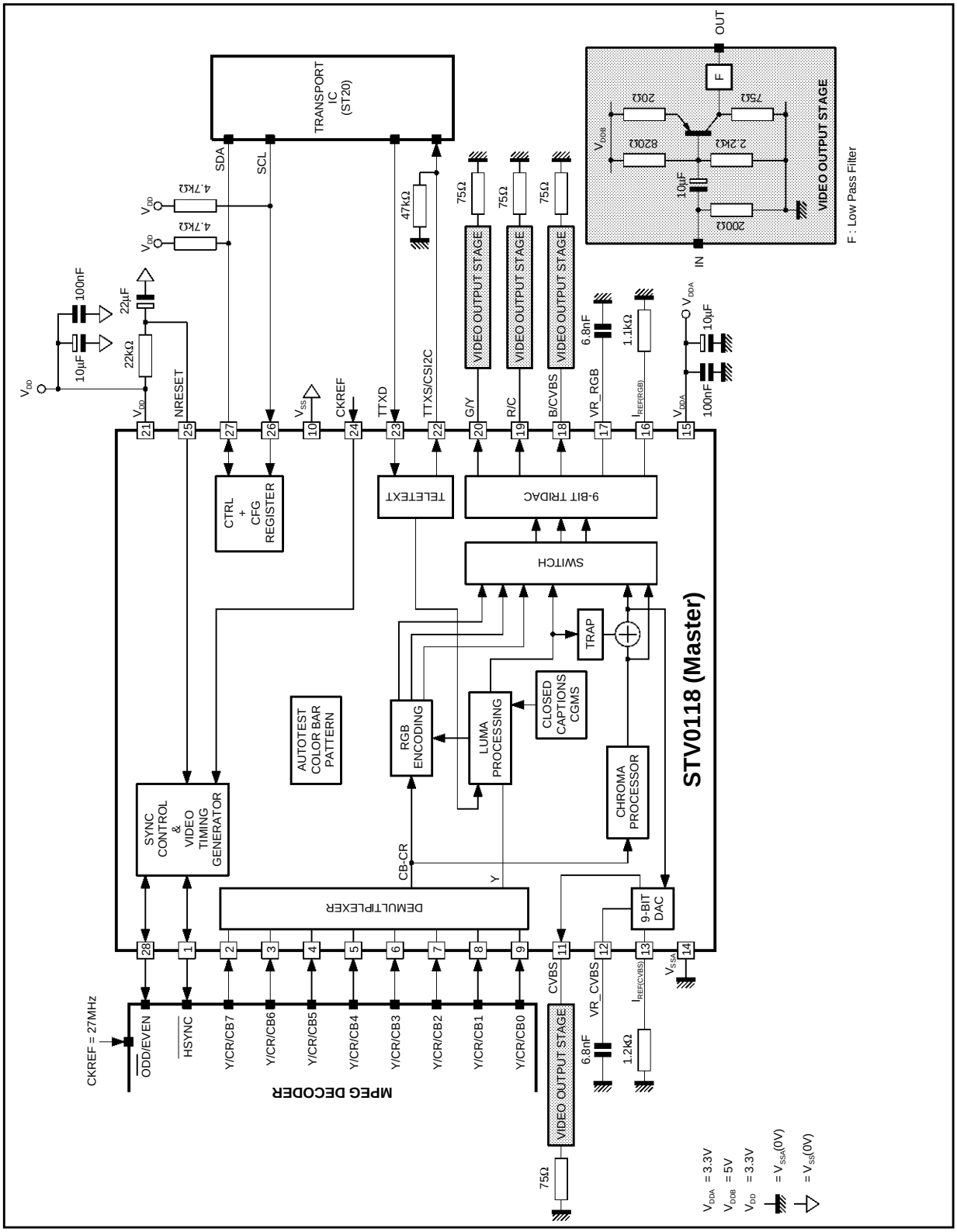
	MSB							LSB
register_44	xxxx	xxxx	xxxx	I2_4	I2_3	I2_2	I2_1	I2_0
Default	0	0	0	0	1	1	1	1

- 525/60 system : (525-SMPTE line number convention)
  Only lines 273 through 284 should be used for closed caption or extended data services (preceding lines contain the vertical sync pulses with equalizing pulses), although it is possible to program over a wider range.
  I2[4:0] = 00000 no line selected for closed caption encoding
  I2[4:0] = 000xx do not use these codes
  I2[4:0] = i line (269 +i) (SMPTE) selected for encoding
  ...
  I2[4:0] = 01111 line 284 (SMPTE) selected for encoding
  I2[4:0] = 11111 line 300 (SMPTE)
  Note : if cgms is allowed on lines 20 and 283 (525/60, 525-SMPTE line number convention), closed captions should not be programmed on these lines.
- 625/50 system : (625-CCIR line number convention)
  Only lines 319 through 336 should be used for closed caption or extended data services (preceding lines contain the vertical sync pulses with equalizing pulses), although it is possible to program over a wider range.
  I2[4:0] = 00000 no line selected for closed caption encoding (i > 0)
  I2[4:0] = i line (318 +i) (CCIR) selected for encoding
  ...
  I2[4:0] = 10010 line 336 (CCIR) selected for encoding
  I2[4:0] = 11111 line 349 (CCIR)
  (*) Default value = 01111 line 284 (525/60, 525-SMPTE line number convention).
  This value also corresponds to line 333 in 625/50 system, (625-CCIR line number convention).

REGISTERS_45 up to 63 : *Reserved*

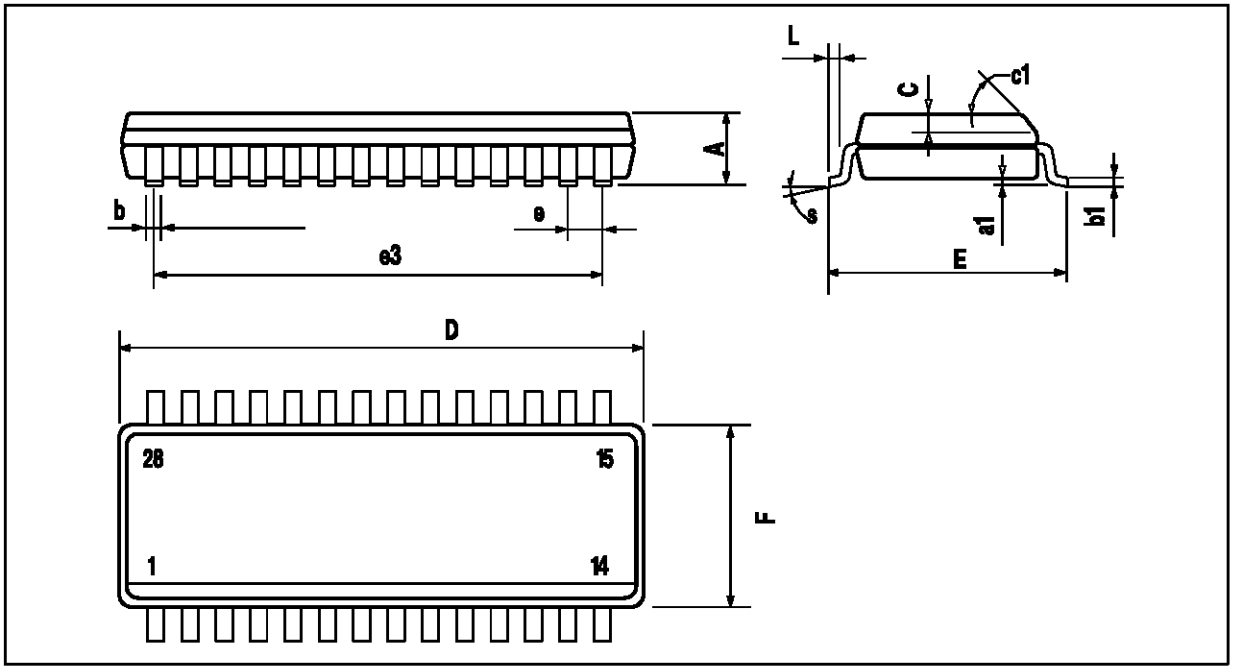
VII - APPLICATION

Figure 34 : Typical Application



VIII - PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.0078
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (Typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (Max.)					

SO28C.TBL